Fundamental Journals
International Journal of Fundamental Physical Sciences (IJFPS)

Original Research Papers
Open Access Journals
ISSN: 2231-8186

IJFPS, Vol 16, No 2, pp 78-91, Jun, 2026
https://doi.org/10.14331/ijfps.2026.330185

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Designing a New Ternary Arithmetic Unit with Overflow Detection Using Reversible Ternary

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Received: Feb 2026
Received in revised: March 2026
Published: Jun 2026

ABSTRACT

Reversible ternary circuit design has attracted considerable attention because ternary logic can reduce interconnection complexity relative to binary logic and is compatible with emerging quantum-computing and nanotechnology platforms. This study proposes a reversible 2-trit ternary parallel adder with a quantum cost of 23, one constant input, and three garbage outputs. Compared with previously reported counterparts, the proposed adder requires lower quantum cost and fewer constant inputs and garbage outputs. Based on this adder, a reversible arithmetic unit is developed for two 2-trit unsigned ternary numbers. The unit performs six arithmetic operations: A+B, A−B, A+1, A−1, A+B+1, and A−B−1. The unsigned inputs and outputs are represented within the decimal range from 0 to 8. A reversible arithmetic unit for two signed 2-trit ternary numbers is also proposed. This circuit has a quantum cost of 32 and requires only one constant input. It performs the same six arithmetic operations using the 3's-complement representation over the range from −4 to +4. In addition, a new reversible overflow detection module is introduced for signed addition and subtraction. By integrating this module with the proposed signed arithmetic unit, a complete reversible ternary arithmetic circuit with overflow-detection capability is obtained. All proposed circuits are constructed using 1-qutrit shift gates and 2-qutrit Muthukrishnan–Stroud gates, which are primitive ternary gates suitable for implementation in ion-trap quantum-computing technology.

Keywords: Quantum computing; reversible ternary logic; ternary parallel adder; reversible arithmetic unit; overflow detection

1 INTRODUCTION

Quantum computing has attracted considerable attention because it offers computational models that differ fundamentally from those of conventional computing. The design of quantum circuits is closely related to reversible logic. In a reversible circuit, the number of outputs equals the number of inputs, and a unique one-to-one correspondence exists between the input and output vectors. Consequently, the input information can, in principle, be reconstructed from the outputs, and no logical information is lost during the computation (Nielsen and Chuang, 2000; Feynman, 1986; Peres, 1985).

Energy dissipation is an important concern in the design of digital circuits (Gershenfeld,1996; Zhirnov et al., 2003). Landauer (1961) demonstrated that the irreversible erasure of one bit of information is associated with a minimum energy dissipation of

$$E_{\min} = k_B T \ln 2, \quad (1)$$

where k_B is the Boltzmann constant and T is the absolute temperature at which the computation is performed. In irreversible computation, information is destroyed during logical operations, resulting in fundamental energy dissipation.

Bennett (1973) subsequently showed that computation can, in principle, be performed reversibly, thereby avoiding the fundamental energy cost associated with logical information erasure. However, practical reversible and quantum-computing systems may still dissipate energy through control, measurement, error correction, and other physical processes.

Ternary logic is one of the most widely studied forms of multivalued logic.

Because each ternary digit can represent three states, a ternary circuit may require fewer signal lines, interconnections, and circuit components than a comparable binary circuit. Consequently, ternary logic can potentially reduce circuit complexity and implementation area (Dhande et al., 2014; Miller and Thornton, 2008; Khan, 2009). It has also been reported that quantum circuits based on reversible ternary logic can be more compact than comparable reversible binary circuits (Khan and Perkowski, 2007; Haghparast et al., 2017). Energy dissipation associated with information loss and the physical area occupied by circuit components are therefore important challenges in integrated-circuit design. One possible approach to addressing these challenges is to combine reversible computing with ternary logic.

A qutrit, or quantum ternary digit, is the fundamental unit of information in ternary quantum computing and can exist in one of the computational basis states 0, 1, or 2. Several physical and theoretical implementations of qutrit-based quantum computers have been investigated (Muthukrishnan and Stroud, 2000; Klimov et al., 2003; McHugh and Twamley, 2005).

Reversible ternary circuits are commonly evaluated using several design parameters, including the number of garbage outputs, the number of constant inputs, and the quantum cost (Khan and Perkowski, 2007).

Garbage outputs: Garbage outputs are circuit outputs that are required to preserve reversibility but are not used as the primary computational results. An efficient reversible circuit should minimize the number of such outputs.

Constant inputs: Constant inputs are input lines that must be initialized to fixed values, such as 0, 1, or 2, to realize the required reversible function. Reducing the number of constant inputs decreases the ancillary-resource requirements of the circuit.

Quantum cost: Quantum cost is commonly defined as the total number of elementary quantum gates required to realize a reversible circuit under a specified gate library and cost model. In this study, the elementary gate library consists of 1-qutrit shift gates and 2-qutrit Muthukrishnan–Stroud (M–S) gates. These gates are regarded as primitive operations in reversible ternary computing and may be implemented using ion-trap-based quantum technologies (Muthukrishnan and Stroud, 2000).

Following the cost convention adopted in the referenced literature, each 1-qutrit shift gate and each 2-qutrit M–S gate is assigned a quantum cost of one (Khan and Perkowski, 2007).

An efficient reversible ternary circuit should therefore minimize its quantum cost, number of constant inputs, and number of garbage outputs while preserving the required functionality and reversibility.

Several reversible ternary adder and subtractor circuits have previously been proposed (Khan and Perkowski, 2007; Monfared and Haghparast, 2016, 2017; Haghparast et al., 2017; Panahi et al., 2018; Lisa and Babu, 2015; Deibuk and Biloshytskyi, 2015; Deibuk, 2016; Monfared and Haghparast, 2017; Panahi et al., 2021; Asadi et al., 2020, 2021). However, comparatively limited attention has been given to complete reversible ternary arithmetic units that support both signed arithmetic and explicit overflow detection. The present study addresses this problem by developing a reversible 2-trit ternary arithmetic unit with overflow-detection capability. The principal contributions of this paper are summarized as follows:

- An efficient reversible 2-trit ternary parallel adder is proposed.
- Reversible ternary arithmetic units are developed for both unsigned and signed 2-trit input numbers.
- A reversible ternary sign-detection circuit and an overflow-detection module are introduced.
- A complete reversible signed ternary arithmetic unit with overflow-detection capability is constructed.

The proposed reversible 2-trit ternary parallel adder is designed to reduce quantum cost, constant inputs, and garbage outputs relative to the selected existing designs. Based on this adder, separate arithmetic units are developed for unsigned and signed ternary numbers. Each arithmetic unit supports the six operations $A+B$, $A-B$, $A+1$, $A-1$, $A+B+1$, and $A-B-1$. For the signed arithmetic unit, the input and output numbers are represented using the 3's-complement system over the range from -4 to $+4$.

To identify invalid results produced when signed addition or subtraction exceeds the representable numerical range, a new reversible overflow-detection module is introduced. This module examines the signs of the operands and the computed result. By integrating the module with the proposed signed arithmetic unit, a complete reversible ternary arithmetic circuit capable of detecting overflow is obtained.

The remainder of this paper is organized as follows. Section 2 introduces the fundamentals of the ternary Galois field, $GF(3)$. Section 3 describes the primitive reversible ternary gates used in the proposed circuits. Section 4 presents the unsigned and signed ternary numeral systems considered in this study. Section 5 explains the arithmetic procedures for signed and unsigned ternary addition and subtraction. Section 6 presents the proposed reversible ternary adder, unsigned arithmetic unit, signed arithmetic unit, sign detector, and overflow-detection module. Section 7 evaluates the proposed circuits and compares them with existing designs where comparable circuits are available. Finally, Section 8 presents the conclusions and directions for future work.

2 TERNARY GALOIS FIELD

Multivalued logic systems can potentially reduce circuit area, hardware complexity, the number of components, and the number of cascaded gates required in digital-circuit design and implementation. A multivalued logic system operates with a radix greater than two. Among such systems, ternary logic is one of the most widely investigated forms of multivalued logic. Because each ternary digit can represent three distinct states, ternary logic can encode more information per digit than binary logic and may therefore reduce the hardware resources required for certain circuit implementations.

A field containing a finite number of elements is called a finite field, or a Galois field. A finite field with p^n elements is denoted by $\mathrm{GF}(p^n)$, where p is a prime number and n is a positive integer. The ternary Galois field, denoted by $\mathrm{GF}(3)$, is defined over the set $\mathrm{GF}(3) = \{0,1,2\}$. Its two fundamental binary operations are addition modulo 3 and multiplication modulo 3. In this paper, these operations are denoted by $\oplus$ and $\odot$, respectively. The field $\mathrm{GF}(3)$ provides the algebraic basis for the design and analysis of reversible ternary quantum circuits.

The addition and multiplication tables of $\mathrm{GF}(3)$ are presented in Table 1. The field operations satisfy the following properties (Panahi et al., 2021; Khan et al., 2005; Łukasiewicz, 1920):

- **Commutative laws:**

$$a \oplus b = b \oplus a, \qquad a \odot b = b \odot a$$

- **Associative laws:**

$$a \oplus (b \oplus c) = (a \oplus b) \oplus c$$
$$a \odot (b \odot c) = (a \odot b) \odot c$$

- **Identity elements:**

$$a \oplus 0 = a \quad , \quad a \odot 1 = a$$

- **Inverse elements:**

$$a \oplus (-a) = 0$$

and, for every nonzero $a \in \mathrm{GF}(3)$,

$$a \odot a^{-1} = 1$$

- **Distributive law:**

$$a \odot (b \oplus c) = (a \odot b) \oplus (a \odot c)$$

Table 1. Addition and multiplication operations in GF(3) (Panahi et al., 2021; Khan et al., 2005).

$\oplus$	**0**	**1**	**2**	$\odot$	**0**	**1**	**2**
0	0	1	2	0	0	0	0
1	1	2	0	1	0	1	2
2	2	0	1	2	0	2	1

3 BASIC REVERSIBLE TERNARY GATES

This section introduces the elementary gates used to construct the proposed reversible ternary circuits. The adopted gate library consists of 1-qutrit shift gates and 2-qutrit Muthukrishnan–Stroud gates.

3.1 Shift Gates

There are six permutation transformations of a single qutrit state. These transformations are elementary reversible ternary gates, each of which is assigned a quantum cost of one under the cost model adopted in this study (Khan and Perkowski, 2007). Their operations are listed in Table 2. These operations are generally referred to as Z-transformations, and the conventional circuit symbol of a shift gate is shown in Fig. 1. The shift gates considered in this study can be classified into two principal categories:

1- Increment gates

The increment gates add either one or two modulo 3 to the input qutrit. The gates $Z(+1)$ and $Z(+2)$ belong to this category and are defined as $Z(+1)(x) = x \oplus 1$ and $Z(+2)(x) = x \oplus 2$, respectively. Their operations are based on addition in $\mathrm{GF}(3)$, as presented in Table 1.

2- Transposition gates

The gates $Z(12)$, $Z(01)$, and $Z(02)$ interchange two ternary states while leaving the third state unchanged. In particular:

- $Z(12)$ interchanges states 1 and 2 while leaving state 0 unchanged;
- $Z(01)$ interchanges states 0 and 1 while leaving state 2 unchanged;
- $Z(02)$ interchanges states 0 and 2 while leaving state 1 unchanged.

As shown in Table 2, every shift gate has a corresponding inverse.

Table 2. Operations of the permutation shift gates (Khan and Perkowski, 2007).

Input	Z	$Z(+1)$	$Z(+2)$	$Z(12)$	$Z(01)$	$Z(02)$
	Buffer	**Single shift**	**Dual shift**	**Transposition**	**Transposition**	**Transposition**
0	0	1	2	0	1	2
1	1	2	0	2	0	1
2	2	0	1	1	2	0

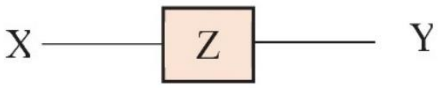

Fig 1. Commonly used circuit symbol for a 1-qutrit shift gate (Khan and Perkowski, 2007).

Applying a gate followed by its inverse restores the original qutrit state. The inverse relationships are summarized in Table 3.

Table 3. Permutation shift gates and their inverse gates (Khan and Perkowski, 2007).

Gate	$Z(+1)$	$Z(+2)$	$Z(12)$	$Z(01)$	$Z(02)$
Inverse gate	$Z(+2)$	$Z(+1)$	$Z(12)$	$Z(01)$	$Z(02)$

3.2 Muthukrishnan–Stroud Gates

Muthukrishnan and Stroud (2000) introduced a primitive 2-qutrit controlled gate for multivalued quantum logic that can be used in reversible ternary circuit design. The schematic representation of a Muthukrishnan–Stroud gate, hereafter referred to as an M–S gate, is shown in Fig. 2.
Let A and B denote the two input qutrits, and let P and Q denote the corresponding outputs. The first input, A, acts as the control qutrit, whereas B is the target qutrit. The gate operation is defined by

$$P = A \tag{2}$$

and

$$Q = \begin{cases} Z(B), & A = 2, \\ B, & A \neq 2, \end{cases} \tag{3}$$

where Z may represent any one of the transformations

$$Z \in \{Z(+1), Z(+2), Z(01), Z(02), Z(12)\}$$

Thus, the selected Z-transformation is applied to the target input B only when the control input is equal to 2. Otherwise, the target qutrit remains unchanged. Under the quantum-cost convention used in this paper, each M–S gate has a quantum cost of one (Khan and Perkowski, 2007).

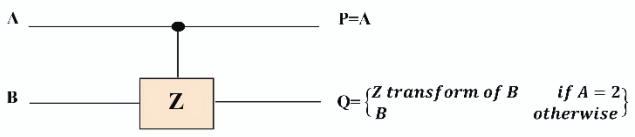

Fig 2. Circuit symbol of a 2-qutrit Muthukrishnan–Stroud gate (Khan and Perkowski, 2007; Muthukrishnan and Stroud, 2000).

THE TERNARY NUMERAL SYSTEM

A suitable numerical representation is required to implement reversible arithmetic operations on integer numbers using ternary logic. In this paper, integer numbers are represented using 2-trit code words. Each element of a ternary code word is called a trit and can take one of the values 0, 1, or 2. Consequently, a 2-trit code can represent

$$3^2 = 9 \tag{4}$$

distinct code words. This section first introduces the representation of unsigned integers and then describes the signed ternary representation used for positive and negative numbers (Dhande et al., 2014).

4.1 Unsigned Ternary Number Representation

In a ternary numeral system, each digit can take one of the values 0, 1, or 2. The positional value of each trit is determined by a power of 3. Therefore, an n-trit ternary number can be converted to its decimal equivalent using

$$(N)_{10} = a_{n-1}3^{n-1} + \cdots + a_2 3^2 + a_1 3^1 + a_0 3^0, \tag{5}$$

where

$$a_i \in \{0,1,2\}.$$

An n-trit code provides 3^n distinct code words. When all code words are used to represent unsigned integers, the representable numerical range is

Table 4. Unsigned 2-trit ternary number representation.

Ternary code	Decimal unsigned number
00	0
01	1
02	2
10	3
11	4
12	5
20	6
21	7
22	8

$$0 \leq N \leq 3^n - 1. \tag{6}$$

In an unsigned ternary representation, the most significant trit does not indicate the sign of the number. For a 2-trit code, the representable decimal range is from 0 to 8. The corresponding code words are listed in Table 4.

4.2 Signed Ternary Number Representation

Several methods can be used to represent signed integers in ternary logic, including sign–magnitude representation, diminished-radix complement, and radix complement. In this paper, the 3's-complement representation is used for signed ternary numbers.

For an n-trit ternary number, the 3's complement of a nonzero number can be obtained in two steps. First, the 2's complement of each trit is calculated by replacing every trit a_i with $2 - a_i$. Then, one is added to the least significant trit using ternary addition. Equivalently, the 3's complement of an n-trit number N can be expressed as

$$3^n - N \tag{7}$$

As an example, consider the representation of -3. The positive decimal number 3 is represented in ternary form as $(3)_{10} = (10)_3$. The digitwise 2's complement of $(10)_3$ is $(12)_3$. Adding one to the least significant position gives

$$(12)_3 + (01)_3 = (20)_3$$

Table 5. Signed 2-trit ternary number representation using the 3's-complement system.

3's-complement ternary code	Decimal signed number
00	0
01	1
02	2
10	3
11	4
12	−4
20	−3
21	−2
22	−1

Therefore,

$$(-3)_{10} = (20)_3$$

in the 2-trit 3's-complement representation. Positive numbers retain the same code as in the unsigned representation. For example, $(+4)_{10} = (11)_3$. For an n-trit 3's-complement representation, the numerical range is symmetric about zero and is given by

$$-\frac{3^n-1}{2} \le N \le +\frac{3^n-1}{2} \tag{8}$$

For $n = 2$, the representable range is therefore

$$-4 \le N \le +4. \tag{9}$$

The complete 2-trit 3's-complement representation is shown in Table 5. For the 2-trit representation considered in this paper, the codes 00, 01, 02, 10, 11 represent the values from 0 to +4, whereas 12, 20, 21, 22 represent the values from −4 to −1.

In particular, $(11)_3$ represents +4, while $(12)_3$ represents −4. Therefore, the most significant trit alone is not sufficient to determine the sign in every case; the complete 2-trit code must be considered.

5 TERNARY ADDITION AND SUBTRACTION

This section describes the procedures used for the reversible addition and subtraction of two 2-trit ternary numbers. The arithmetic procedures are first explained for unsigned numbers and then for signed numbers represented in the 3's-complement system.

The conditions under which overflow occurs are also discussed. Overflow occurs when the exact result of an arithmetic operation lies outside the numerical range that can be represented by the adopted code. In such a case, the output code does not represent the correct mathematical result (Dhande et al., 2014).

5.1 Unsigned 2-Trit Addition and Subtraction

The addition of two unsigned 2-trit ternary numbers is performed by adding the corresponding trits and propagating any carry from the least significant position to the most significant position. For example,

$$(10)_3 + (12)_3 = (22)_3 \tag{10}$$

which corresponds to $3 + 5 = 8$. Because the maximum unsigned value representable by two trits is 8, overflow occurs whenever the exact addition result exceeds 8. Such an overflow can be identified using the carry-out from the most significant trit. For example,

$$(12)_3 + (20)_3 = (102)_3 \tag{11}$$

When only two result trits are retained, the output is $(02)_3$ with a carry-out of 1. Since $5 + 6 = 11 > 8$, the two-trit result is invalid, and the carry-out indicates the occurr ence of unsigned overflow.

Subtraction can be implemented by adding the minuend to the 3's complement of the subtrahend. Thus,

$$A - B = A + \mathrm{Comp}_3(B) \tag{12}$$

where $\mathrm{Comp}_3(B)$ denotes the 3's complement of B. If a carry-out of 1 is produced during unsigned subtraction, the result is nonnegative. In that case, the carry-out is discarded, and the remaining 2-trit code is the magnitude of the result.

If no carry-out is produced, the intermediate output is a negative number represented in 3's-complement form.

The 3's complement of this intermediate code must then be calculated to obtain the unsigned magnitude, while a separate sign output indicates that the result is negative.

Example 1.

Consider the subtraction $6-4=2$. The ternary representations are $6=(20)_3$, $4=(11)_3$. The 3's complement of $(11)_3$ is $(12)_3$.
Therefore,

$$(20)_3+(12)_3=(102)_3 \tag{13}$$

After discarding the carry-out, the result is $(02)_3=2$. Thus, the correct result is $+2$.

Example 2.

Consider the subtraction $3-6=-3$. The ternary codes are$3=(10)_3, 6=(20)_3$. The 3's complement of $(20)_3$ is $(10)_3$. Therefore,

$$(10)_3+(10)_3=(20)_3 \tag{14}$$

No carry-out is generated, indicating a negative result. The intermediate result $(20)_3$ is the 3's-complement representation of -3.
To obtain the unsigned magnitude, the 3's complement of $(20)_3$ is calculated: $\mathrm{Comp}_3((20)_3)=(10)_3$. Hence, the result is $-(10)_3=-3$.
Subtraction of two unsigned 2-trit numbers does not produce overflow when a separate sign output is available, because the magnitude of the difference always lies between 0 and 8.

5.2 Signed 2-Trit Addition and Subtraction

In this study, signed ternary numbers are represented using the 3's-complement system. The addition of two signed 2-trit ternary numbers can be performed using the same 2-trit ternary adder used for unsigned numbers.
Any carry-out from the most significant trit is discarded. For the adopted 2-trit signed representation, the valid numerical range is $-4 \le N \le +4$.
Overflow occurs whenever the exact result lies outside this range. In signed addition, overflow occurs when two operands having the same sign produce a result whose sign is opposite to that of the operands.

Example 1.

Consider $(-4)+(-3)=-7$. The corresponding 3's-complement codes are $-4=(12)_3, -3=(20)_3$. The ternary addition gives

$$(12)_3+(20)_3=(102)_3 \tag{15}$$

After discarding the carry-out, the 2-trit output is $(02)_3$, which represents $+2$. This result is invalid because the exact result, -7, is outside the representable range.

The two negative operands have produced an apparently positive output, thereby indicating signed overflow.
Signed subtraction is performed by adding the minuend to the 3's complement of the subtrahend:

$$A-B=A+\mathrm{Comp}_3(B) \tag{16}$$

The same signed-overflow principle applies after the subtraction has been converted into addition. In particular, overflow occurs when the two effective addends have the same sign and the computed result has the opposite sign.

Example 2.

Consider $(-3)-(+2)=-5$. The exact result, -5, lies outside the representable range from -4 to $+4$. The corresponding ternary codes are $-3=(20)_3, +2=(02)_3$. The 3's complement of $(02)_3$ is $(21)_3$, which represents -2. Therefore,

$$(20)_3+(21)_3=(111)_3 \tag{17}$$

After discarding the carry-out, the 2-trit output is $(11)_3$, which represents $+4$. Since two negative effective addends have produced a positive result, overflow has occurred. The code $(11)_3$ must therefore not be interpreted as the correct result of the subtraction.

6 PROPOSED REVERSIBLE CIRCUITS

This section presents reversible parallel circuits for the addition and subtraction of two signed or unsigned 2-trit ternary integers. Subtraction is implemented by adding the 3's complement of the subtrahend to the minuend. In addition to the basic operations $A+B$ and $A-B$, the proposed arithmetic circuits perform

$$A+1, \qquad A-1, \qquad A+B+1, \qquad A-B-1$$

Separate arithmetic units are developed for unsigned and signed ternary numbers. A reversible sign-detection circuit and a new overflow-detection module are also introduced. By integrating the overflow-detection module with the signed arithmetic unit, the proposed circuit can identify invalid results produced when the exact value of a signed addition or subtraction lies outside the representable range from -4 to $+4$.
All proposed circuits are constructed using 1-qutrit shift gates and 2-qutrit Muthukrishnan–Stroud gates.
These gates form the primitive reversible ternary gate library adopted in this study and have been considered for physical realization in ion-trap-based quantum-computing technologies.

6.1 Proposed Reversible 2-Trit Unsigned Ternary Adder

This subsection presents the proposed reversible parallel adder for two unsigned 2-trit ternary numbers. The circuit implementation is shown in Fig. 3.

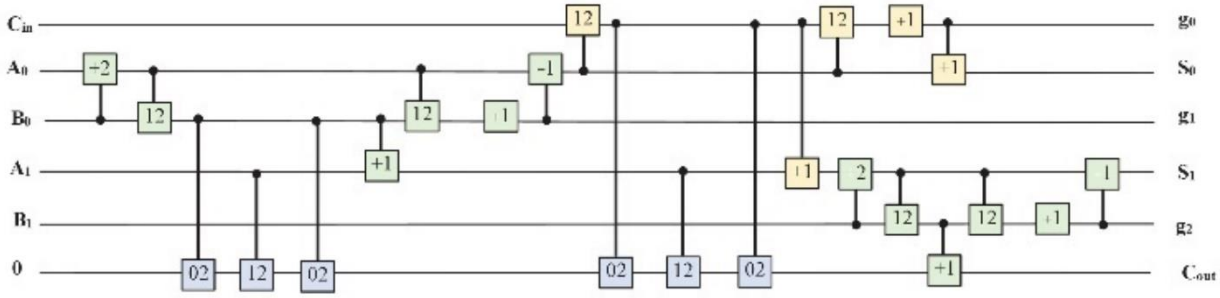

Fig 3. Implementation of the proposed reversible 2-trit unsigned ternary parallel adder.

The two input operands are denoted by

$$A = (A_1A_0)_3 \qquad \text{and} \qquad B = (B_1B_0)_3$$

where A_1 and B_1 are the most significant trits, while A_0 and B_0 are the least significant trits. The circuit also receives an input carry C_{in}. Its principal outputs are the 2-trit sum $S = (S_1S_0)_3$ and the carry-out C_{out}.

The proposed circuit is implemented using 20 M–S gates and three 1-qutrit shift gates. Under the quantum-cost model adopted in this study, its total quantum cost is therefore

$$\text{QC} = 20 + 3 = 23 \tag{18}$$

Only one constant input is required. The input carry C_{in} may be assigned either 0 or 1, depending on the required arithmetic operation. Compared with the reversible ternary parallel adders reported in Refs. (Khan and Perkowski, 2007; Haghparast et al., 2017; Lisa and Babu, 2015; Deibuk, 2016; Monfared and Haghparast, 2017; Asadi et al., 2020, 2021), the proposed design requires lower quantum cost and fewer ancillary resources.

In unsigned 2-trit addition, a carry-out of $C_{\text{out}} = 1$ indicates that the exact sum exceeds the representable range from 0 to 8. In this case, unsigned overflow has occurred, and the retained 2-trit result alone is not a valid representation of the exact sum.

6.2 Proposed Reversible 2-Trit Unsigned Ternary Arithmetic Unit

This subsection presents the proposed reversible arithmetic unit for two unsigned 2-trit ternary numbers. The circuit implementation is shown in Fig. 4, and its supported arithmetic operations are summarized in Table 6.

Table 6. Arithmetic operations performed by the proposed circuit in Fig. 4.

S	$C_{\text{in}}/B_{\text{in}}$	Input A	Input B	Operation
0	0	A	B	$A + B$
0	1	A	B	$A + B + 1$
0	1	A	$(00)_3$	$A + 1$
0	0	A	$(22)_3$	$A - 1$
2	0	A	B	$A - B$
2	1	A	B	$A - B - 1$

The control input S determines whether the circuit performs addition or subtraction, while $C_{\text{in}}/B_{\text{in}}$ selects the corresponding increment or borrow condition. When $S = 0$, the circuit operates as an adder and performs functions based on the circuit introduced in Fig. 3. When $S = 2$, the circuit operates in subtraction mode. To calculate $A - B$, the control values are selected as

$$S = 2, \qquad C_{\text{in}} = 0$$

The 3's complement of B is first generated and then added to A. Thus, subtraction is implemented according to

$$A - B = A + \text{Comp}_3(B) \tag{19}$$

If $A \geq B$, the result is nonnegative. In this case, the output $\text{Sign}/B_{\text{out}}$ is equal to 0, and the resulting magnitude is represented by a valid unsigned ternary code in the range from 0 to 8.

If $A < B$, the mathematical result is negative. In this case, the intermediate output is produced in 3's-complement form, and the output $\text{Sign}/B_{\text{out}}$ is equal to 1. The 3's complement of the intermediate result is then calculated to obtain the unsigned magnitude of the difference.

The two input operands are always unsigned numbers in the range from 0 to 8. The output magnitude also lies within this range, while the separate sign output indicates whether the result is positive or negative. Therefore, subtraction of two unsigned 2-trit integers does not produce magnitude overflow because $-8 \leq A - B \leq +8$.

The proposed unsigned arithmetic unit is implemented using 36 M–S gates and seven shift gates. Its quantum cost is therefore

$$\text{QC} = 36 + 7 = 43 \tag{20}$$

The circuit requires two constant inputs initialized to zero.

6.3 Proposed Reversible 2-Trit Signed Ternary Arithmetic Unit

The circuit proposed in this subsection performs addition and subtraction on two signed 2-trit ternary numbers. Its implementation is shown in Fig. 5. The general operation of

this circuit is similar to that of the unsigned arithmetic unit shown in Fig. 4. The principal difference is that the inputs and outputs of the unsigned circuit represent numbers from 0 to 8, whereas the signed circuit operates on numbers in the range from -4 to $+4$.

The signed operands and results are represented using the 3's-complement code presented in Table 5. Subtraction is implemented by adding the 3's complement of the subtrahend to the minuend:

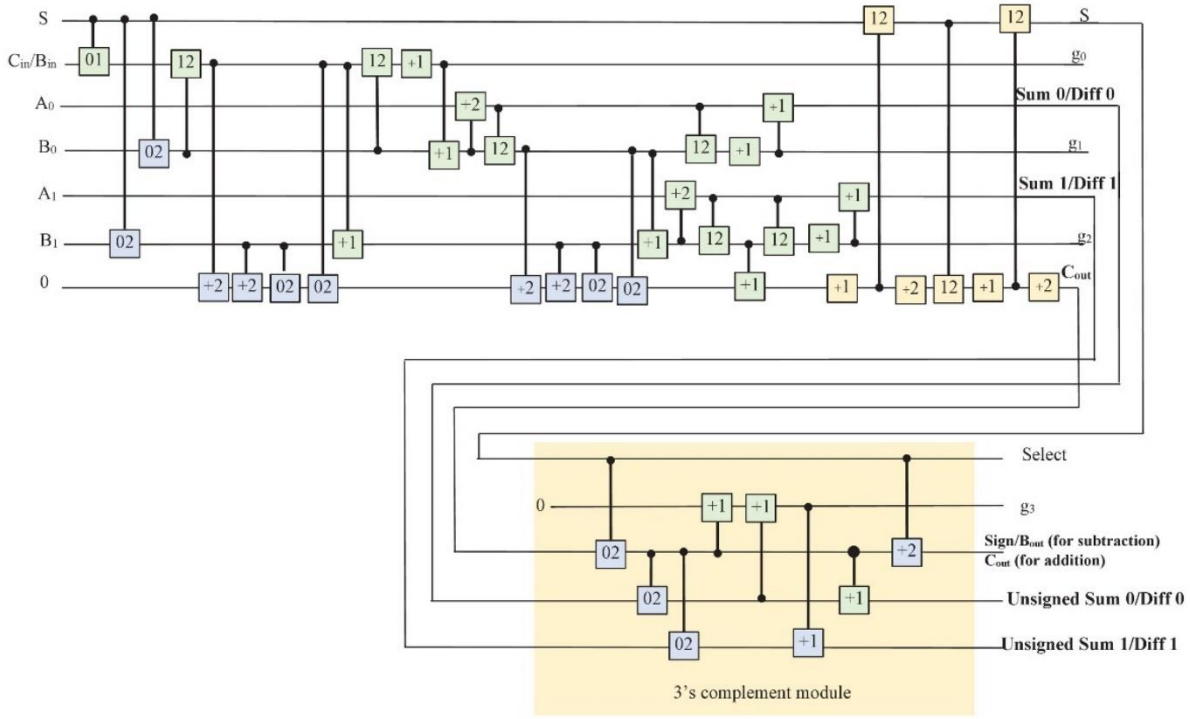

Fig 4. Implementation of the proposed reversible 2-trit unsigned ternary arithmetic unit.

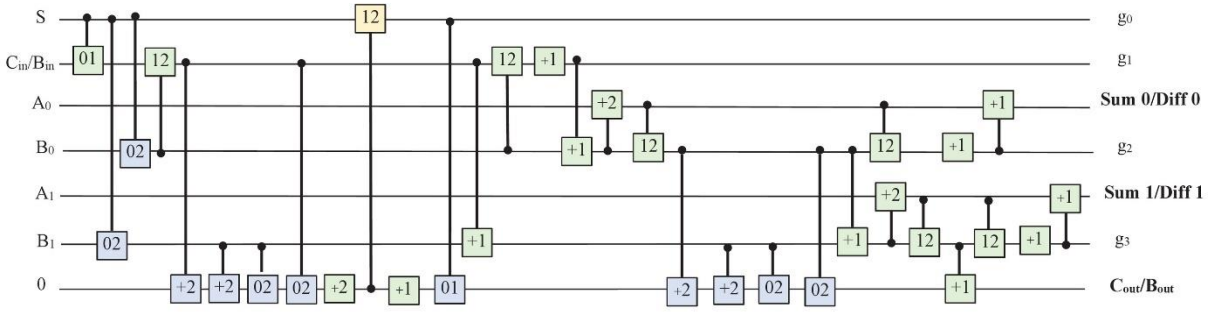

Fig 5. Implementation of the proposed reversible 2-trit signed ternary arithmetic unit.

$$A - B = A + \mathrm{Comp}_3(B) \tag{21}$$

The sign of B does not require separate treatment before complementing because the 3's-complement operation produces the additive inverse of the represented code. The resulting addition or subtraction output remains in 3's-complement representation. The signed arithmetic unit performs all six operations listed in Table 6:

$A + B,$ $A - B,$ $A + 1,$ $A - 1,$ $A + B + 1,$ $A - B - 1$

The circuit is implemented using 27 M–S gates and five shift gates. Its total quantum cost is therefore

$$\mathrm{QC} = 27 + 5 = 32 \tag{22}$$

Only one constant input initialized to zero is required.

6.4 Proposed Reversible Overflow-Detection Module

This subsection introduces a reversible ternary module for detecting overflow in signed addition and subtraction. Because

subtraction is implemented by addition of the 3's complement of the subtrahend, the same overflow-detection principle can be applied to both operations. For an effective addition of two signed operands, overflow occurs when both operands have the same sign but the computed result has the opposite sign. In logical form, the overflow condition can be expressed as

$$\text{Overflow} = (s_A = s_B) \wedge (s_R \neq s_A) \quad (23)$$

where s_A, s_B, and s_R denote the signs of operands A, B, and the computed result, respectively. The proposed module, shown in Fig. 6, examines the signs of the two effective addends and the resulting sum.

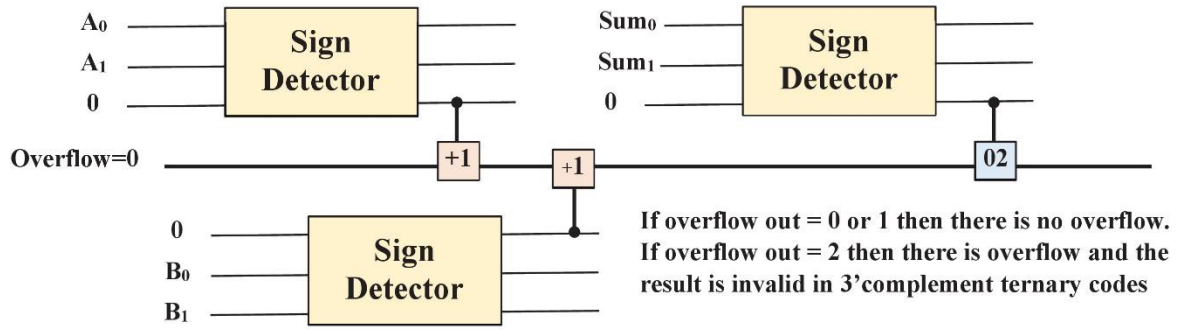

Fig 6. Implementation of the proposed reversible overflow-detection module.

An overflow output equal to 2 indicates that overflow has occurred and that the resulting ternary code does not represent the correct mathematical result. Output values of 0 or 1 indicate that no overflow has occurred.

The overflow-detection module contains three sign-detector blocks: one for operand A, one for operand B, and one for the arithmetic result. For the 2-trit 3's-complement representation adopted in this work, the code words are divided into positive and negative sets as follows:

$$\mathcal{P} = \{(00)_3, (01)_3, (02)_3, (10)_3, (11)_3\} \quad (24)$$

and

$$\mathcal{N} = \{(12)_3, (20)_3, (21)_3, (22)_3\} \quad (25)$$

Accordingly:

- If the most significant trit is 0, the represented number is nonnegative.
- If the most significant trit is 2, the represented number is negative.
- If the most significant trit is 1, the least significant trit must also be examined. The codes $(10)_3$ and $(11)_3$ represent $+3$ and $+4$, respectively, whereas $(12)_3$ represents -4.

Therefore, the most significant trit alone is not sufficient to determine the sign of every 2-trit code. The complete input code must be considered by the sign-detector circuit. The sign detector shown in Fig. 7 generates an output equal to 2 when the input code represents a negative number. For nonnegative inputs, its output is either 0 or 1.

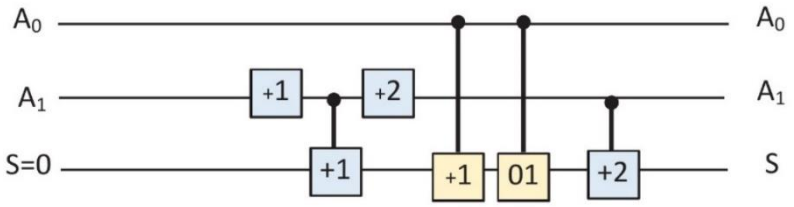

Fig 7. Implementation of the proposed reversible sign-detector module. The output is equal to 2 when the input code represents a negative number and is equal to 0 or 1 when the input code represents a nonnegative number.

The possible combinations of operand signs and result signs are presented in Table 7.

Overflow occurs only in the two cases where the operands have identical signs and the result has the opposite sign. The sign-detector block is implemented using four M–S gates and two shift gates. Its quantum cost is therefore

$$\text{QC}_{\text{sign}} = 4 + 2 = 6 \quad (26)$$

It also requires one constant input initialized to zero. The complete overflow-detection module uses three sign-detector blocks together with the additional gates required to compare their outputs. It is implemented using 15 M–S gates and six shift gates, resulting in a quantum cost of

$$\text{QC}_{\text{overflow}} = 15 + 6 = 21 \quad (27)$$

The complete module requires four constant inputs.

Table 7. Overflow conditions for the effective addition of two signed ternary numbers.

Sign of A	Sign of B	Sign of $A+B$	Overflow output
+	+	+	0
+	+	−	2
+	−	+	1
+	−	−	1
−	+	+	1
−	+	−	1
−	−	+	2
−	−	−	0

Note: An overflow output equal to 2 indicates that overflow has occurred. Overflow is detected when the two effective input operands have the same sign and the computed result has the opposite sign.

6.5 Proposed Reversible 2-Trit Signed Arithmetic Unit with Overflow Detection

The complete reversible signed ternary arithmetic unit is obtained by integrating the overflow-detection module shown in Fig. 6 with the signed arithmetic unit shown in Fig. 5. The resulting circuit is presented in Fig. 8.

The complete unit operates on positive and negative 2-trit numbers represented in the 3's-complement system and performs all six arithmetic operations listed in Table 6.

It additionally determines whether the exact signed result lies outside the representable interval $-4 \leq R \leq +4$.

When the overflow output is equal to 2, the arithmetic output code must be regarded as invalid because the exact mathematical result cannot be represented using the adopted 2-trit signed code. When the overflow output is 0 or 1, the arithmetic output is within the representable range.

The complete circuit is implemented using 59 M–S gates and 21 shift gates. Its total quantum cost is therefore

$$QC = 59 + 21 = 80 \tag{28}$$

The circuit requires seven constant inputs and produces nine garbage outputs.

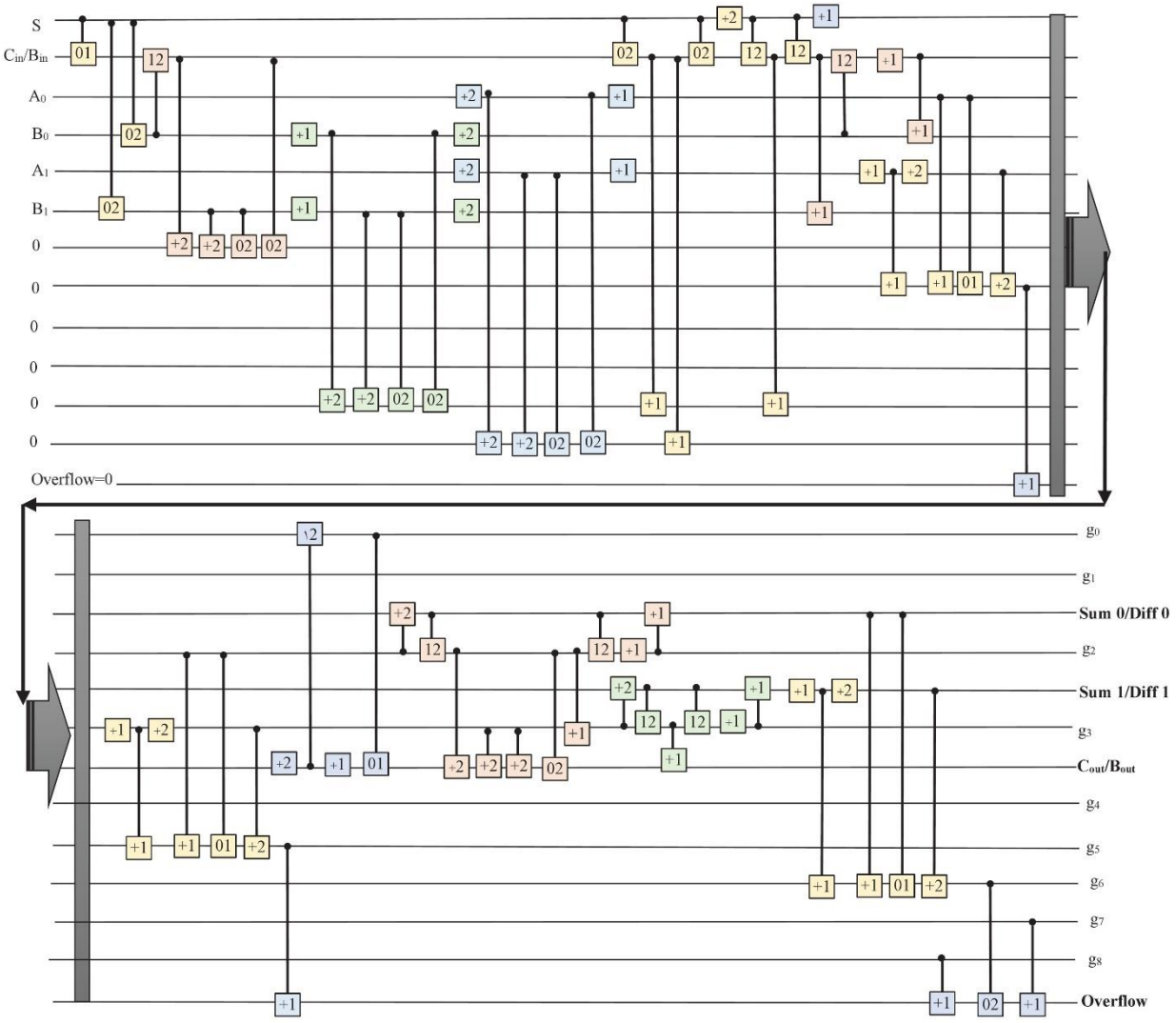

Figure 8. Implementation of the proposed reversible 2-trit signed ternary arithmetic unit with overflow-detection capability.

7 EVALUATIONS OF THE PROPOSED CIRCUITS

This section evaluates the proposed reversible ternary circuits and compares them with previously reported designs wherever directly comparable circuits are available. The principal evaluation criteria are quantum cost, number of constant inputs, number of garbage outputs, and numbers of shift and M–S gates. Under the cost model adopted in this study, a circuit requiring fewer of these resources is generally considered more efficient, provided that the compared circuits implement equivalent functions.

7.1 Evaluation of the Proposed Reversible 2-Trit Unsigned Ternary Adder

Table 8 compares the proposed reversible 2-trit unsigned ternary parallel adder with the existing designs reported in Refs. (Khan and Perkowski, 2007; Haghparast et al., 2017; Lisa and Babu, 2015; Deibuk, 2016; Monfared and Haghparast, 2017; Asadi et al., 2020, 2021). The comparison includes quantum cost, numbers of shift and M–S gates, constant inputs, and garbage outputs.

As shown in Table 8, the proposed circuit has a quantum cost of 23, requires one constant input, and produces three garbage outputs. Among the listed designs, these values are the lowest for the three principal resource measures.

In particular, the use of only one constant input reduces the ancillary-input requirement relative to the previously reported circuits.

7.2 Evaluation of the Proposed Reversible 2-Trit Unsigned Ternary Arithmetic Unit

The proposed unsigned arithmetic unit performs addition and subtraction on two unsigned 2-trit ternary operands. It also supports the six arithmetic functions listed in Table 6. Its principal features are summarized as follows:

- It performs the six operations

$$A + B, \quad A - B, \quad A + 1, \quad A - 1, \quad A + B + 1, \quad A - B - 1$$

Table 8. Comparison of reversible 2-trit unsigned ternary parallel adders.

Design	Garbage outputs	Constant inputs	Shift gates	M–S gates	Quantum cost
Existing design (Khan and Perkowski, 2007)	9	8	28	72	100
Existing design (Monfared and Haghparast, 2017)	8	6	16	52	68
Existing design (Lisa and Babu, 2015)	4	2	24	28	52
Existing design (Haghparast et al., 2017)	4	2	8	20	28
Existing design (Deibuk, 2016)	4	2	8	18	26
Existing design (Asadi et al., 2020)	4	2	4	20	24
Existing design (Asadi et al., 2021)	4	2	4	20	24
Proposed design	3	1	3	20	24

Table 9. Resource analysis of the proposed reversible 2-trit unsigned ternary arithmetic unit.

Design	Garbage outputs	Constant inputs	Shift gates	M–S gates	Quantum cost
Proposed unsigned arithmetic unit	2	5	7	36	43

Table 10. Comparison of reversible 2-trit signed ternary adder/subtractor circuits.

Design	Garbage outputs	Constant inputs	Shift gates	M–S gates	Quantum cost
Existing design (Khan and Perkowski, 2007)	10	9	28	75	103
Existing design (Monfared and Haghparast, 2017)	9	7	16	55	71
Existing design (Lisa and Babu, 2015)	5	3	24	31	55
Proposed design	4	1	5	27	32

- It includes a correction circuit that converts an intermediate negative result from 3's-complement form into an unsigned ternary magnitude in the range from 0 to 8.
- It provides a separate Sign/B_{out} output to indicate the sign of the subtraction result.
- It requires 36 M–S gates and seven shift gates, resulting in a quantum cost of 43.

A directly equivalent previously reported circuit implementing the complete set of functions and the same output-correction mechanism was not identified among the selected references. Therefore, Table 9 reports the resource requirements of the proposed circuit without claiming a direct numerical advantage over functionally different designs.

7.3 Evaluation of the Proposed Reversible 2-Trit Signed Ternary Arithmetic Unit

The proposed signed arithmetic unit operates on positive and negative 2-trit ternary numbers represented in the 3's-complement system. Its inputs and outputs correspond to the codes listed in Table 5, covering the numerical range from -4 to $+4$.

Table 10 compares the proposed signed arithmetic unit with selected reversible ternary parallel adder/subtractor circuits reported in Refs. (Khan and Perkowski, 2007; Lisa and Babu, 2015; Monfared and Haghparast, 2017). The proposed design requires 27 M–S gates and five shift gates, giving a quantum cost of 32. It also requires one constant input and produces four garbage outputs.

For the designs listed in Table 10, the proposed circuit has the lowest reported quantum cost, number of constant inputs, and number of garbage outputs. These reductions indicate lower logical-resource requirements under the common gate-cost model used in the comparison.

7.4 Evaluation of the Proposed Reversible Overflow-Detection Module

The proposed overflow-detection module is composed of three reversible sign-detector blocks and additional gates that combine their outputs according to the signed-overflow condition. Table 11 presents the resource requirements of one sign-detector block and the complete overflow-detection module.

Table 11. Resource analysis of the proposed reversible sign-detector block and overflowdetection module.

Design	Garbage outputs	Constant inputs	Shift gates	M–S gates	Quantum cost
Sign-detector block	2	1	2	4	6
Overflow-detection module	6	4	6	15	21

A sign-detector block requires four M–S gates, two shift gates, one constant input, and produces two garbage outputs. Its total quantum cost is 6. The complete overflow-detection module requires 15 M–S gates and six shift gates, resulting in a quantum cost of 21. It uses four constant inputs and produces six garbage outputs.

Because no directly equivalent reversible ternary overflow-detection circuit was identified among the selected references, Table 11 reports the resource requirements of the proposed design without a direct numerical comparison.

7.5 Evaluation of the Proposed Reversible 2-Trit Signed Arithmetic Unit with Overflow Detection

The complete signed arithmetic unit is obtained by integrating the proposed overflow-detection module with the reversible 2-trit signed ternary arithmetic unit. The resulting circuit performs the six arithmetic operations listed in Table 6 and indicates whether the exact result lies outside the representable interval from -4 to $+4$.

The complete circuit requires 59 M–S gates and 21 shift gates. Its total quantum cost is therefore

$$\mathrm{QC} = 59 + 21 = 80 \tag{29}$$

The circuit also requires seven constant inputs and produces nine garbage outputs. These resource requirements are summarized in Table 12.

A directly equivalent reversible 2-trit signed ternary arithmetic unit with an integrated overflow-detection output was not identified among the selected designs. Consequently, the resource values are reported as an analysis of the proposed circuit rather than as evidence of global optimality.

Table 12. Resource analysis of the proposed reversible 2-trit signed ternary arithmetic unit with overflow detection.

Design	Garbage	Design	Garbage	Design	Garbage
Proposed complete arithmetic unit	7	9	21	59	80

CONCLUSION

This paper presented a reversible ternary arithmetic architecture for signed and unsigned 2-trit numbers. The proposed circuits support the six operations

$$A + B, \quad A - B, \quad A + 1, \quad A - 1, \quad A + B + 1, \quad A - B - 1$$

The designs were constructed using 1-qutrit shift gates and 2-qutrit Muthukrishnan–Stroud gates under a quantum-cost model that assigns a unit cost to each primitive gate.

The proposed reversible 2-trit unsigned ternary parallel adder has a quantum cost of 23, uses one constant input, and produces three garbage outputs. Relative to the selected comparable designs, it requires lower quantum cost and fewer constant inputs and garbage outputs.

Based on this adder, an unsigned ternary arithmetic unit was developed for input numbers ranging from 0 to 8. The circuit includes a correction mechanism for converting negative subtraction outputs from 3's-complement form into an unsigned magnitude and uses a separate output to indicate the sign of the result. The unsigned arithmetic unit has a quantum cost of 43.

A signed ternary arithmetic unit was also presented for operands represented in the 2-trit 3's-complement system over the range from -4 to $+4$. This circuit has a quantum cost of 32, requires one constant input, and produces four garbage outputs. For the comparable designs considered in this study, it provides reduced logical-resource requirements.

A further contribution is the reversible overflow-detection module. The module examines the signs of the two effective operands and the arithmetic result. It produces an overflow output equal to 2 when operands having the same sign generate a result with the opposite sign. The overflow-detection module has a quantum cost of 21.

By integrating this module with the signed arithmetic unit, a complete reversible 2-trit ternary arithmetic circuit with overflow-detection capability was obtained. The complete circuit has a quantum cost of 80, requires seven constant inputs, and produces nine garbage outputs.

An overflow indication identifies cases in which the exact arithmetic result lies outside the representable range and the computed 2-trit output must therefore be regarded as invalid.

The results demonstrate that the proposed designs provide compact logical building blocks for reversible ternary arithmetic. Nevertheless, the present work is limited to 2-trit operands and evaluates the circuits primarily through logical gate counts and quantum cost. Further validation through exhaustive simulation, circuit-depth analysis, physical gate decomposition, and larger operand sizes would strengthen the assessment of their practical applicability.

8.1 Potential Applications and Future Directions

The proposed arithmetic unit may serve as a building block for larger reversible ternary data-processing systems. Potential areas of application include the following:

- **Ternary quantum arithmetic:** Multi-qutrit algorithms that require addition, subtraction, increment, and decrement operations may employ arithmetic units derived from the proposed architecture.
- **Modular arithmetic:** Overflow and range detection can assist in the construction of reversible modular-arithmetic circuits, provided that suitable modular-reduction stages are incorporated.
- **Quantum signal-processing architectures:** Arithmetic building blocks are required in several numerical and signal-processing procedures. Ternary implementations may offer alternative resource trade-offs relative to binary realizations.
- **Ternary error-control systems:** Reversible arithmetic components may support encoding, decoding, or syndrome-processing operations in systems based on ternary symbols.
- **Larger reversible ternary arithmetic logic units:** The proposed designs can provide a basis for the development of multi-trit adders, subtractors, and complete ternary arithmetic logic units.

Future research should extend the proposed circuits to larger operand sizes, including 4-trit and 8-trit architectures. Further work should also investigate carry-propagation delay, circuit depth, nearest-neighbour constraints, ancilla restoration, physical decomposition costs, and exhaustive verification of all possible input combinations. Optimization of the overflow-detection circuitry and integration into a complete reversible ternary arithmetic logic unit are additional directions for future study.

AVAILABILITY OF DATA AND MATERIALS

All data and circuit information supporting the findings of this study are included in the article

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