Fundamental Journals
International Journal of Fundamental Physical Sciences (IJFPS) ISSN:2231-8186
IJFPS, Vol 4, No 4, pp 122-126, Dec , 2014 ***Y.K. Sharma***
DOI:10.14331/ijfps.2014.330076
http://dx.doi.org/10.14331/ijfps.2014.330076

Electrical Properties of the 3C-SiC/SiO_2 Interface Grown With High Temperature Oxidation

Y.K. Sharma[1]*, F. Li, C.A. Fisher[1], M.R. Jennings[1], A. Perez-Tomas[2], S.M. Thomas[1], D. Hamilton[1] and P.A. Mawby[1]

[1] School of Engineering, University of Warwick, Coventry, United Kingdom
[2] Institut Català de Nanociència i Nanotecnologia (ICN2), Campus de la UAB,
Edifici ICN2 08193, Bellaterra (Barcelona), Catalonia, Spain

Y.K.Sharma@warwick.ac.uk
(*Received Oct 2014; Published Dec 2014*)

ABSTRACT

3C-Silicon carbide (SiC) metal-oxide-semiconductor (MOS) capacitors are fabricated to study the 3C-SiC/SiO_2 interface using standard hi-low capacitance-voltage (C-V) and conductance-voltage (G-V) methods. Devices are fabricated on an n-type 3C-SiC epilayer grown on a (100) oriented silicon (Si) substrate. Dry oxidation is done at different temperatures (1200°C - 1400°C) to grow the oxide layer. The 1300°C as-oxidized device gives the lowest D_{it} of $5.8 \times 10^{11} eV^{-1} cm^{-2}$ at 0.25eV away from the conduction band (CB) edge. SIMS and AFM analyses of the devices have shown that there is no detrimental effect of high temperature oxidation on the oxide stoichiometry and surface roughness.

Keywords: SiC, AFM, high temperature oxidation, interface trap density, C-V, G-V, bias-stress

DOI:10.14331/ijfps.2014.330076

INTRODUCTION

In order to save energy on the national electric power grid, the idea of redesigned 'micro-grids' has been proposed (Hatziargyriou, Asano, Iravani, & Marnay, 2007; Lasseter & Paigi, 2004). For this we need power devices which can operate at higher switching speeds and block voltages of up to 20kV (Zhang et al., 2010). A potential solution for this problem is to employ power devices fabricated using a wide band gap semiconductor material such as silicon carbide. Silicon carbide (SiC) is a wide band gap semiconductor, and has more than 200 polytypes. Out of different polytypes, hexagonal (6H-and 4H-) and cubic (3C-) polytypes are of particular interest to fabricate power devices (Roccaforte et al., 2014; Sharma et al., 2013). Due to higher band gap of the 4H-compared to 3C-, it is not possible to fabricate an efficient power MOSFET for voltages less than 1kV. This is due to the poor interface properties of the 4H-SiC after dry (thermal) oxidation (Afanas' ev, 1999). Unlike, SiC the oxidation of Si leads to an abrupt interface and the defects formed (Si dangling bonds) during oxidation can be passivated via hydrogen passivation. Typically, a post-oxidation annealing process is used to improve the interface properties of the 4H-SiC/SiO_2 interfaces. This process is known as the interface passivation process (Li, Dimitrijev, Harrison, & Sweatman, 1997; Modic et al., 2014; Okamoto, Yano, Hirata, Hatayama, & Fuyuki, 2010; Sharma et al., 2014; Sharma et al., 2012). With all these advances the cost is still a big concerned and keeping 4H-SiC technology away from realizing its full potential. With the 3C-SiC, it is possible to grow 3C-SiC on the Si substrate. And as a result it is possible to reduce the cost of SiC devices. Also, due to smaller band gap of the 3C-SiC, it is well-suited for 1kV voltage range power devices. In this work, dry oxidation is performed at different temperatures (1200^{oC}, 1300°C and 1400^{oC}) to grow the oxide. The oxidation process is discussed in a greater detail somewhere else (Thomas, Jennings, Sharma, Fisher, & Mawby, 2014). Previous studies have shown that high-temperature oxidation (≥ 1400^{oC}) reduces the interface trap density (D_{it})in 4H-MOS capacitors, but has not been tried yet on 3C-SiC MOS (metal oxide capacitor) devices. The highest temperature that had been used to grow the interface on 3C-SiC in literature is 1250^{oC} (Constant et al., 2011; Esteve, Schoner, Reshanov, Zetterling, & Nagasawa, 2009; Kondo, Takahashi, Ishii, Hayashi, & Sakuma, 1986). The hi-low C-V technique is used to extract the interface trap density (D_{it}) (Shenoy et al., 1995). It is found that the 1300^{oC} dry oxidation process resulted in a lowest D_{it} of $6\times10^{11}eV^{-1}cm^{-2}$. In addition to C-V technique, GV measurements are performed to analysis the interface. The G-V curves at higher frequencies (>1kHz) showed an increase in the measured conductance (G), indicating the presence of traps which are energetically far away from the CB edge. Because of the wide band gap of 3C-SiC compared to Si these traps exhibit extremely large emission times at room temperature. Also, each of the devices is stressed in depletion for different time intervals. For long stressing hours a hook is observed and is less visible in the case of 1300^{oC} oxidation process.

MATERIALS AND METHODS

The material used in this study was purchased from NOVASIC Inc. To fabricate lateral MOS capacitors we have used 3C-SiC/Si wafer with heterostructure grown on-axis p-type Si (001) substrate. The 3C-SiC epilayer was grown with MOCVD with an n-type unintentional doping concentration of $\leq 1\times10^{16}$ cm^{-3}, and is 10μm thick. Lateral circular MOS capacitors with diameter of 300μm had been used in this study. Device fabrication started with standard organic and Radio Corporation of America (RCA) to degrease the sample and other source of contamination (alkali ions, metal impurities). After this, thermal oxidation was done at aforementioned temperatures. The oxide thicknesses of these samples were in the range of 60-70 nm and measured from accumulation capacitance. Photolithography was used to define the device pattern. And finally e-beam evaporator was used to deposit a 400nm of Al, to make gate contacts.

RESULTS AND DISCUSSION

Fig. 1 shows the hi-low C-V curves and interface trap density extracted for various devices. For the C-V curves, there is a large flatband voltage shift (ΔV_{FB}) toward negative gate bias The flatband voltage shift shows the existence of net positive fixed charge at the interface and its origin is the presence of carbon-clusters and dangling bonds formed after thermal oxidation. Also, we can see that the 1300^{oC} as-oxidized MOS capacitor gives the lowest D_{it}. The 1400^{oC} has the second best D_{it}, and 1200^{oC} device has the highest D_{it}. In the case of 1200^{oC} process the D_{it} is considerably higher as we go deeper into the energy band gap. Although, D_{it} for the 1400°C MOS capacitor start increasing as we go deeper into the energy band gap (higher than 0.35eV). Atomic force microscopy (AFM) analysis is done on all the devices to see the effect of temperature on the surface morphology. And results are shown in Fig. 2, 0.53nm-0.62nm. G-V curves for these devices are shown in Fig. 3. The area under the conductance peak is a measure of D_{it} (Nicollian, Brews, & Nicollian, 1982). These results again confirm that the 1300°C oxidation process gives an improved interface. The peak conductance occurs at flatband voltage (V_{FB}) corresponding to E_c-E = 0.25eV.

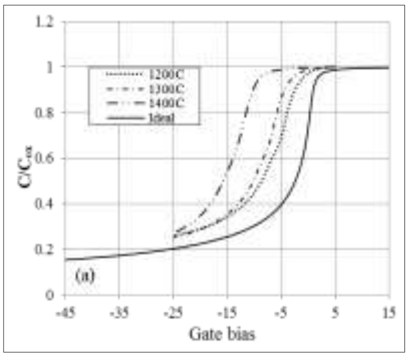


Fig1. (a) High frequency (100kHz) C-V data for different metal-oxide-semiconductor (MOS) capacitors

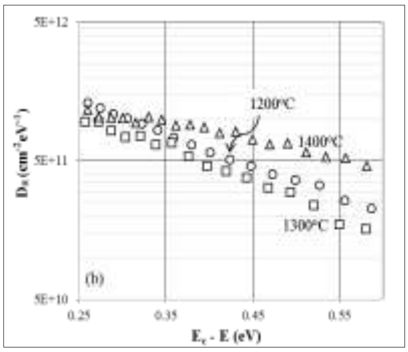
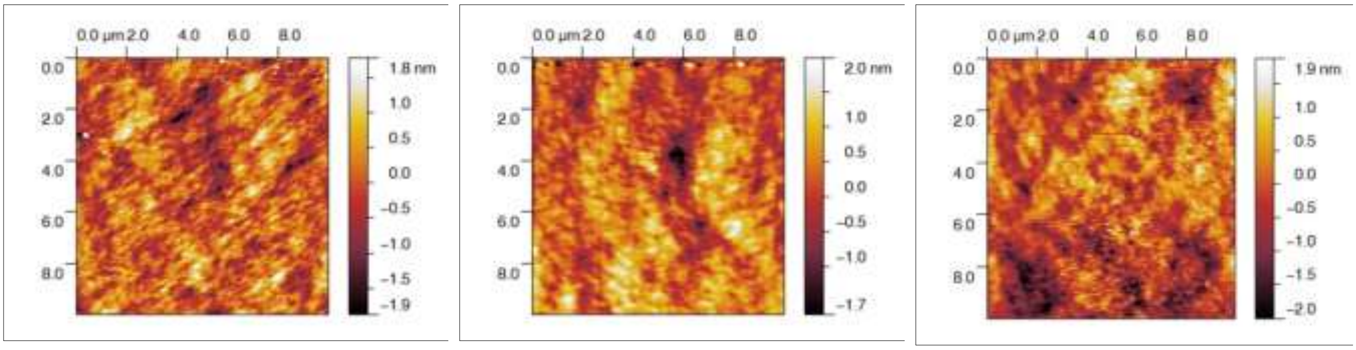


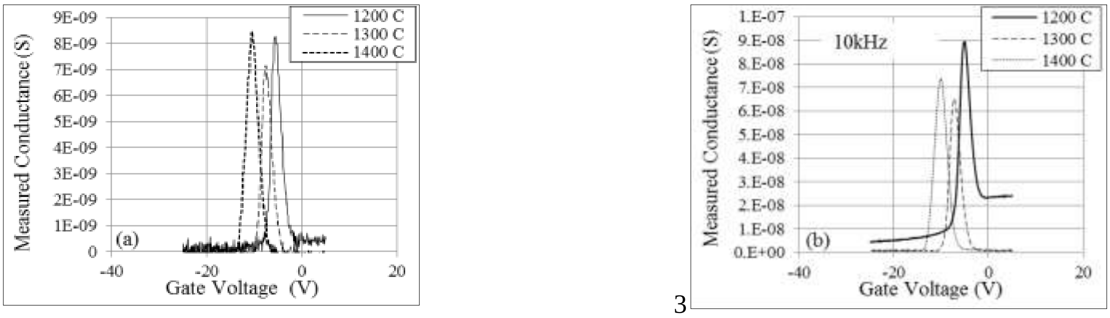
Fig. 1(b) Interface trap density for MOS capacitors after room temperature hi-low CV technique.



(a) T = 1200^{oC} **(b)** T = 1300^{oC} **(c)** T = 1400^{oC}

Fig 2. Atomic force microscopy(AFM) results for the MOS capacitor grown at different temperature

Devices with the interface grown at 1200^{oC} and 1400^{o}C have lager area under the G-V curves compared with 1300^{oC}, implying higher D_{it} for these devices. There is a large increase in the conductance for higher frequencies at positive gate voltages, indicating the presence of a second type of traps which are sensitive to higher frequencies at room temperature(Krieger et al., 2008). All the G-V curves have a finite full width at half maximum (FWHM) suggesting that these traps are distributed over a finite energy range in the energy band gap. Also, at 1MHz there is an increase in the conductance value for positive bias, this observation indicates that there is a second type of traps which are sensitive to only 1MHz frequency. These traps are present at different energy position in bandgap and have different electrical capture-cross-section and time constant compared to traps which can be detected only at 100kHz



(a) ω = 1 kHz **(b)** ω = 10 kHz

(c) ω = 100 kHz **(d)** ω = 1MHz

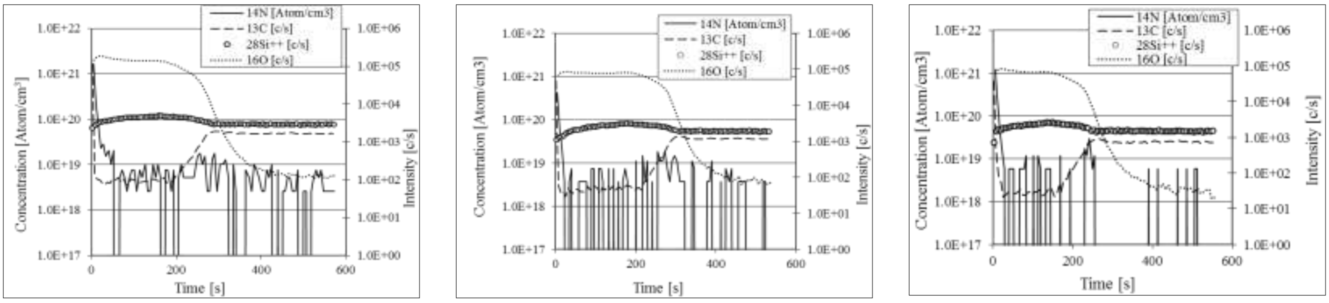
Fig 3. G-V curves of *3C-SiC MOS* structures taken for different gate biases at probe frequency (ω)

Some of the important parameters for these devices are listed in Table I. In addition to deep depletion and a hysteresis, all the CV curves in Fig. 5 are strongly shifted towards negative voltages. This can be attributed to the fact that the effective charge (Q_{EFF}) for the MOS capacitors is positive. Fixed oxide charge (Q_F), oxide trapped charges (Q_{OT}) mobile ions (Q_M) are the constituent of Q_{EFF}. The flatband voltage for these devices is negative; and is highest for the 1400^{o}C oxidation process. The negative V_{FB} means that the net effective charge is positive, and the values are listed Table I. And is calculated using the following simple relation; Q_{EFF} $(cm^{-2})/q = \Delta V_{FB} \times C_{OX}/q$. Also, all the C-V curves for the devices have a distinctive bump corresponding to filled surface states which cannot be discharged either by capture or emission processes. This phenomenon has been observed in the case of Si MOS capacitors at low temperatures (Goetzberger & Irvin, 1968).

Table 1. Detailed experimental conditions used to fabricate 3C-SiC MOS structures. Oxide thickness (Tox), flat band voltage (VFB), and QEFF/q of investigated MOS capacitors.

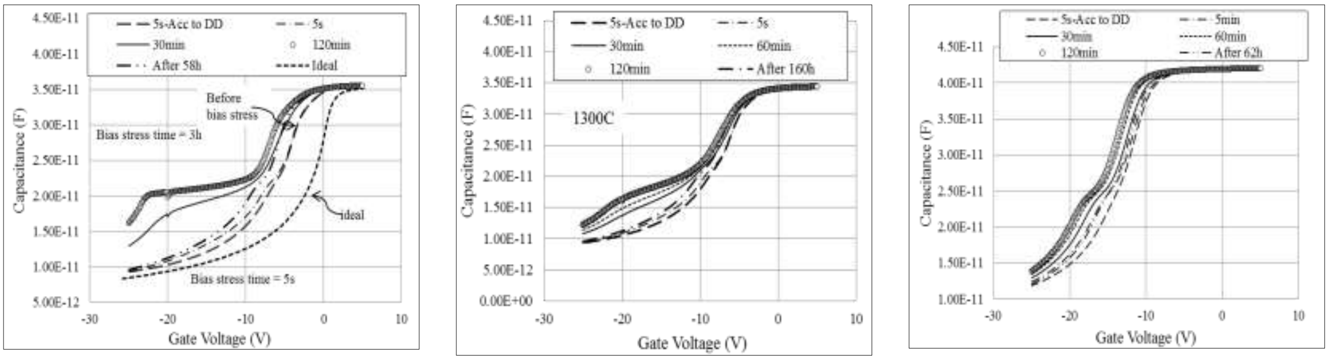
Device	Oxide	$T^{(oC)}$	Gas species	Flow rate (l/min)	Oxide thickness, T_{ox} (nm)	Flat band voltage V_{FB} (V)	Effective oxide charge, Q_{EFF}/q (cm^{-2})
1	Thermal	1200	O_2	4	68.21	-4	1.07×10^{12}
2	Thermal	1300	O_2	4	72.74	-6	1.06×10^{12}
3	Thermal	1400	O_2	4	59.65	-12	4.13×10^{12}

The Secondary ion mass spectrometry (SIMS) profiles are shown in Fig. 4. There is virtually no significant difference between the Si, O and C profiles for all the devices, and it could be due to no out-diffusion or diffusion of species from the interface. To characterize the interface further, hi-low CV measurements are performed in depletion for different stress times ($T = 5\,s$, 5min, 2h, and 3h etc.) for all the MOS capacitors. Results for the 1200^{o}C oxidation are shown in Fig. 5(a). Before performing the stressing experiment a normal C-V sweep is done from accumulation (A)-depletion (D)-accumulation (A). Results are shown in Fig. 5(a) with dotted (A) and solid (D) red lines, and correspond to a small hysteresis effect. And this is due to slow nature of near-interface traps. In depletion, if the stressing time is ≥60min, a ledge of constant capacitance is observed (Berberich, Godignon, Locatelli, Millan, & Hartnagel, 1998). This could be due to a delayed evacuation of minority carriers resulted from high band bending in deep depletion and/or is a consequence of charge carrier dynamics and depends on minority carrier generation at the 3C-SiC/SiO$_2$ interface. After this the device was relaxed for 58h but the C-V curve is still shifted to the left as compared its original position. This is due to the de-trapping of some of the minority carriers which are generated during the formation of the ledge.



(a) T=1200^{oC} **(b)** at T=1300^{oC} **(c)** at T=1400^{oC}

Fig 4. SIMS profiles for a 3C-SiC MOS capacitor fabricated at different temperatures



(a) T = 1200^{oC} **(b)** T = 1300^{oC} **(c)** T = 1400^{oC}

Fig 5. High frequency, 1MHz, C-V curves for a *3C-SiC MOS* capacitor with oxide grown at different temperatures

Similar behaviour is observed for the 1300^{oC} as-oxidized MOS capacitor. The ledge formed in this case is different as compared with 1200^{oC} as-oxidized MOS capacitor and has higher slope. This is due to the presence of higher Q_{EFF}/q (1.60×10^{12}), resulting in a reduced electric field at the inreface. Consequentially, it is difficult to generate minority carriers in depeltion under biased stress condtion. Also in this case even after relaxing the device for more than 58h, the C-V curve does not come back to its orginal postion. In the case of 1400^{oC} device it is hard to get into deep depeltion because of very high postive charge (4.13×10^{12}) at the interface. The hi-low C-V measurements have shown that this device gives the highest D_{it} and therefore has not been consdiered for futher analysis.

CONCLUSION

High temperature oxidation is used to grow the 3C-SiC/SiO2. Out of all the temperatures 1300°C as-oxidized gives lowest Dit of $6\times10^{11}eV^{-1}cm^{-2}$ at 0.25eV. Hi-low C-V and G-V techniques are used to characterize the interface and all of them give consistent results. The results reported here for the novel high temperature oxidation. SIMS and AFM analysis have shown that the high-temperature oxidation process does change the stoichiometry and surface roughness. The biased stress experiments have shown thatched devices underwent 1200^{oC} oxidation goes to inversion due to the generation of minority carriers as compared to other devices. Also, even after relaxing the devices for ling hour after stressing the C-V curves never come back to their original position, showing that lot of carriers are still trapped. Although, there is an increase in the net positive charge at the interface with increasing oxidation temperature, which is contrary to the previous reported results and needs further analysis.

ACKNOWLEDGMENT

This project, Vehicle Electrical Systems Integration (VESI), was funded by the Engineering and Physical Sciences Research Council (ESPRC), (Grant # RESEE-3065). The authors would also like to thank Dr. Mark Crouch and Dr. S. E Burrows for their help during this project. Also, the authors gratefully acknowledge the Nano-Si group, Department of Physics, University of Warwick for use of their electrical characterization facilities.

REFERENCES

Afanas' ev, V. (1999). Electronic properties of SiO2SiC interfaces. *Microelectronic engineering, 48*(1), 241-248.

Berberich, S., Godignon, P., Locatelli, M.-L., Millan, J., & Hartnagel, H. (1998). High frequency< i> CV</i> measurements of SiC MOS capacitors. *Solid-State Electronics, 42*(6), 915-920.

Constant, A., Camara, N., Placidi, M., Decams, J.-M., Camassel, J., & Godignon, P. (2011). Interfacial properties of oxides grown on 3C-SiC by rapid thermal processing. *Journal of The Electrochemical Society, 158*(1), G13-G19.

Esteve, R., Schoner, A., Reshanov, S., Zetterling, C.-M., & Nagasawa, H. (2009). Advanced oxidation process combining oxide deposition and short postoxidation step for N-type 3C-and 4H-SiC. *Journal of applied physics, 106*(4), 044514-044514-044515.

Goetzberger, A., & Irvin, J. (1968). Low-temperature hysteresis effects in metal-oxide-silicon capacitors caused by surface-state trapping. *Electron Devices, IEEE Transactions on, 15*(12), 1009-1014.

Hatziargyriou, N., Asano, H., Iravani, R., & Marnay, C. (2007). Microgrids. *Power and Energy Magazine, IEEE, 5*(4), 78-94.

Kondo, Y., Takahashi, T., Ishii, K., Hayashi, Y., & Sakuma, E. (1986). Experimental 3C-SiC MOSFET. *IEEE electron device letters, 7*, 404-406.

Krieger, M., Beljakowa, S., Trapaidze, L., Frank, T., Weber, H., Pensl, G., Schöner, A. (2008). Analysis of interface trap parameters from double-peak conductance spectra taken on N-implanted 3C-SiC MOS capacitors. *physica status solidi (b), 245*(7), 1390-1395.

Lasseter, R. H., & Paigi, P. (2004). *Microgrid: a conceptual solution.* Paper presented at the Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual.

Li, H.-f., Dimitrijev, S., Harrison, H. B., & Sweatman, D. (1997). Interfacial characteristics of N 2 O and NO nitrided SiO 2 grown on SiC by rapid thermal processing. *Applied physics letters, 70*(15), 2028-2030.

Modic, A., Sharma, Y., Xu, Y., Liu, G., Ahyi, A., Williams, J., Dhar, S. (2014). Nitrogen Plasma Processing of SiO2/4H-SiC Interfaces. *Journal of Electronic Materials, 43*(4), 857-862.

Nicollian, E. H., Brews, J. R., & Nicollian, E. H. (1982). *MOS (metal oxide semiconductor) physics and technology* (Vol. 1987): Wiley New York et al.

Okamoto, D., Yano, H., Hirata, K., Hatayama, T., & Fuyuki, T. (2010). Improved inversion channel mobility in 4H-SiC MOSFETs on Si face utilizing phosphorus-doped gate oxide. *Electron Device Letters, IEEE, 31*(7), 710-712.

Roccaforte, F., Fiorenza, P., Greco, G., Vivona, M., Lo Nigro, R., Giannazzo, F., Saggio, M. (2014). Recent advances on dielectrics technology for SiC and GaN power devices. *Applied Surface Science, 301*, 9-18.

Sharma, Y., Ahyi, A., Isaacs-Smith, T., Modic, A., Park, M., Xu, Y., Williams, J. (2013). High-mobility stable 4H-SiC MOSFETs using a thin PSG interfacial passivation layer. *IEEE Electron Device Lett, 34*(2), 175-177.

Sharma, Y., Ahyi, A., Issacs-Smith, T., Modic, A., Xu, Y., Garfunkel, E., Fan, L. (2014). Advancements in SiC power devices using novel interface passivation processes *Physics of Semiconductor Devices* (pp. 47-52): Springer.

Sharma, Y., Ahyi, A., Issacs-Smith, T., Shen, X., Pantelides, S., Zhu, X., Williams, J. (2012). Phosphorous passivation of the SiO< sub> 2</sub>/4H–SiC interface. *Solid-State Electronics, 68*, 103-107.

Shenoy, J., Chindalore, G., Melloch, M., Cooper, J., Palmour, J., & Irvine, K. (1995). Characterization and optimization of the SiO2/SiC metal-oxide semiconductor interface. *Journal of Electronic Materials, 24*(4), 303-309.

Thomas, S. M., Jennings, M. R., Sharma, Y. K., Fisher, C. A., & Mawby, P. A. (2014). *Impact of the Oxidation Temperature on the Interface Trap Density in 4H-SiC MOS Capacitors.* Paper presented at the Materials Science Forum.

Zhang, Q., Callanan, R., Das, M., Ryu, S.-H., Agarwal, A. K., & Palmour, J. W. (2010). SiC power devices for microgrids. *Power Electronics, IEEE Transactions on, 25*(12), 2889-2896.