Noname manuscript No.
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Designing a new ternary arithmetic unit with overflow detection using reversible ternary gates

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Received: date / Accepted: date

Abstract Added to the advantages of the ternary logic application as opposed to binary logic, such as reducing the complexity of interconnects, and consistent with its application within the quantum computer and other technologies associated with the nanotechnology domain, reversible ternary circuit design is now being taken into consideration. This study sought to propose a new reversible 2-trit ternary parallel adder with a quantum cost of 23 and one constant input. When compared with the existing counterparts, the proposed circuit has lower quantum cost and constant inputs. Subsequently, the reversible ternary arithmetic circuit for six mathematical operations calculation of A+B, A-B, A+1, A-1, A+B+1 and A-B-1 for two 2-trit unsigned ternary numbers was proposed. In the proposed unsigned arithmetic circuit, two input numbers and the obtained results were coded in unsigned ternary representation ranging from 0 to 8. Next, the reversible ternary arithmetic circuit for two 2-trit signed ternary numbers with the quantum cost of 32 and one constant input was proposed. The proposed signed arithmetic circuit, similar to the proposed unsigned arithmetic, can be used to calculate six mathematical operations of A+B, A-B, A+1, A-1, A+B+1 and A-B-1; and in comparison with existing counterparts, it had lower quantum cost and constant inputs. In the proposed signed arithmetic circuit, two input numbers and the obtained results were in 3's complement representation ranging from -4 to +4. What follows is an introduced new module for detecting the overflow occurrence for signed numbers adding and subtracting calculations, and by adding it to the proposed reversible signed ternary arithmetic circuit, the overflow detection capability was provided for this circuit. All the proposed circuits were implemented using 1-qutrit shift gates and 2-qutrit MS gates which are primitive ternary gates in quantum computers and can be implemented in ion-trap technology.

Keywords Quantum Computers · Reversible Ternary Logic · Parallel Adder · Reversible Arithmetic Unit

1 Introduction

Currently, as opposed to conventional computer types, it is of high significance to recognize the quantum computer supremacy and dominance, especially in terms of their ability to multitask the commands accomplishment. The primary logic leading to quantum computers and their computing circuit design is reversible logic. Circuits, based on such logic, have the same number of inputs and outputs, and there is a unique one-to-one mapping between inputs and outputs. Therefore, no information is lost in these circuits. Accordingly, A circuit with such a capability is called the reversible circuit [1–3].

Heat generation is one of the most important issues in the digital circuit design [4, 5]. In 1960, Landauer [6] proved that, despite the use of high technology in the design of digital circuits in any irreversible calculation, for any data bit loss, $KTLn2$ joule of thermal energy is produced. (K denotes the Boltzmann's constant and T represents the absolute temperature at which computation is performed). Accordingly, considering all the irreversible technologies, the initial values are destroyed and cannot be recovered; and the results of which would be heat generation when implementing the calculation. Bennet, in 1973 [7], showed that if a digital circuit had a reversible design, heat would not be theoretically produced.

The use of ternary logic is more applicable in multi-valued logic. The number of inputs and outputs of the circuit designed in ternary logic is less than the similar designed in binary logic, so the complexity

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of the designed circuit is reduced [8–10]. Quantum circuits designed using reversible ternary logic would be 37% more compact than other similarly designed circuits in reversible binary logic [11, 17].

Therefore, the heat generation for each bit of data loss and the lack of area occupied in the chip are two key challenges in the design of integrated circuits. One of the strategies to reduce these challenges is to integratively use reversible and ternary logic in circuit design.

A qutrit (quantum ternary digit) is a unit of information in reversible ternary logic and it can be one of the numbers of 0, 1 and 2. The designs of qutrit quantum computer are provided in Refs. [12–14]. The ternary reversible circuits performance can be evaluated in terms of the number of garbage outputs, constant inputs and quantum cost [11].

Garbage Outputs: The garbage outputs refer to logical functions which are not used as the approved outputs. To maintain the reversibility in the reversible circuits garbage outputs are added.

Constant Inputs: The constant inputs refer to the number of inputs which must be constant at 0 or 1 or 2 in order to achieve the desired reversible logic functions.

Quantum cost: Quantum cost refers to the number of primitive gates including 1-qutrit shift gates and 2-qutrit M-S gates. Shift and MS gates are primitive gates in quantum/reversible ternary computing which are implemented in liquid ion-trap quantum technology [12]. The quantum cost of each of these gates is 1 [11].

The reversible ternary logic circuit is an efficient design with the minimum number of garbage outputs, minimum quantum cost and minimum number of constant inputs.

Different designs for reversible ternary adder and subtractor circuits have been proposed in Refs. [11, 15–25]. In reversible ternary logic, the circuit design for arithmetic unit with overflow detection capability has not yet been studied and evaluated.

The highlights of this paper are summarized as follows:

- Introducing an efficient reversible 2-trit ternary parallel adder
- Introducing a reversible ternary parallel arithmetic unit with two signed/unsigned inputs numbers
- Introducing a reversible ternary module to detect the presence of overflow
- Proposing an arithmetic unit with overflow detection capability

In this paper, a novel design for the reversible ternary arithmetic unit with overflow detection capability for two 2-trit signed input numbers has been proposed. In the proposed circuit, we tried to design a circuit with the least quantum cost if possible. For fulfilling such purpose, a new integration circuit for the reversible 2-trit ternary parallel adder was proposed. Compared with the existing counterparts, our proposed parallel adder has less quantum cost, fewer number of constant inputs and garbage outputs. Using our proposed parallel adder, new designs for reversible ternary parallel arithmetic are first presented for two unsigned inputs and then for the two signed inputs. To detect the presence of overflow as a result of calculating the addition and subtraction of two signed numbers, a new module is proposed so that the overflow detection capability is provided in the addition and subtraction calculation of signed numbers by applying the new module in the our proposed reversible arithmetic.

The structure of the paper is as follows: Section 2 explains the basis of ternary circuit design (GF3). In section 3 the primitive reversible ternary gates used in this paper are introduced. The ternary numeral systems which are used in this study are presented in section 4. In section 5, the mathematical calculations comprising the addition and subtraction for the numeral systems which are used in this study for the signed and unsigned numbers are explained. Section 6 shows our proposed reversible ternary circuits realization including new reversible parallel ternary adder, reversible parallel unsigned ternary adder/subtractor, reversible parallel signed ternary adder/subtractor and new module for overflow detection in addition/subtraction on signed numbers. All of which are used to construct our proposed reversible parallel signed ternary arithmetic unit with overflow detection. In Section 7, the proposed circuits evaluation is discussed. Finally, the conclusion of our work is provided in Section 8.

2 Ternary galois field

The use of multi-level logic systems can reduce the chip area, complexity, system components and number of cascaded gates in the digital circuits design and implementation. A multi-level system operates on a radix higher than two. Ternary logic is a very promising system in multi-valued logic (MVL). The main advantage of the ternary system in comparison to the binary system is that it displays more information with the same digits. So, using a ternary logic system can reduce hardware complexity.

A field that contains a limited number of elements is called a finite field. Galois field (GF) can be considered as a special case of a finite field. The number of elements in the GF(p^n) is in the form of p^n, in which p is the prime number and n is the positive integer.

Ternary Galois Field 3 (GF3) is an algebraic structure defined on the set of{0,1,2} with two basic binary operations, the first one is the addition module 3 and the other one is the multiplication module 3. GF3 serves as the foundation for the design and construction of reversible ternary quantum circuits. The truth table of ternary GF3 addition ($\oplus$) and multiplication ($\odot$) operations are shown in table 1. GF3 operations satisfy the following axioms [23, 26, 27]:

- Commutative law: $a \oplus b = b \oplus a$, $a \odot b = b \odot a$
- Associative law: $a \oplus (b \oplus c) = (a \oplus b) \oplus c$, $a \odot (b \odot c) = (a \odot b) \odot c$
- Identity element: $a \oplus 0 = a$, $a \odot 1 = a$
- Inverse element: $a \oplus (-a) = 0$, $a \odot a^{-1} = 1$
- Distributive law: $a \odot (b \oplus c) = (a \odot b) \oplus (a \odot c)$

Table 1 Galois field 3 addition and multiplication operations [23, 26].

($\oplus$)	0	1	2	($\odot$)	0	1	2
0	0	1	2	0	0	0	0
1	1	2	0	1	0	1	2
2	2	0	1	2	0	2	1

3 Basic Reversible Ternary Gates

In this section, the basic gates (shift and MS gates) in reversible ternary circuit design are explained.

3.1 Shift gates

There are six permutative transforms of qutrit states, which are elementary gates with the quantum cost of one [11]. Table 2 shows the operations of the permutative gates. This is known as a Z-transformation and the symbol in quantum circuits is shown in Fig. 1.

These gates can be divided into two categories according to their function.

1. Incremental gates:
   In these gates, one or two units are added to the input value. Gates Z(+1) and Z(+2) are in this category. As a result using these gates adds one or two units to the input value, respectively. The addition operation in these gates is based on Table 1 in Galois field.
2. Replacement gates:
   In this type of gates, the input value is replaced by one of the values 0, 1 or 2. Gates Z(12) and Z(02) are in this category. In gate Z(12), if the input value is 1, it will be replaced by a value of 2, and if the input value is 2, it will be replaced by a value of 1. In gate Z(01), if the input value is 0 or 1, it is replaced with 1 or 0, respectively. In gate Z(02), it is replaced with 2 or 0, respectively, only if the input value is 0 or 2. As can be seen from the function of these gates, the input value of 0 in gate Z(12), the input value of 1 in gate Z(02) and the input value of 2 in gate Z(01) will not change.

Considering the shift gates functioning in Table 2, it is noticeable that each gate has an inverse gate; accordingly, if it is used consecutively, it will result in the same initial input. Table 3 presents the inverse gates for each shift gate.

Table 2 Permutative gates operations [11]

Input	Z	Z(+1)	Z(+2)	Z(12)	Z(01)	Z(02)
	Buffer	Single-Shift	Dual-Shift	Self-Shift	Self-Single Shift	Self-Dual Shift
0	0	1	2	0	1	2
1	1	2	0	2	0	1
2	2	0	1	1	2	0

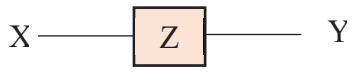

Fig. 1 The commonly used symbol for shift gates [11].

Table 3 Permutative gates and their inverse gates [11]

gate	Z(+1)	Z(+2)	Z(12)	Z(01)	Z(02)
Inverse gate	Z(+2)	Z(+1)	Z(12)	Z(01)	Z(02)

3.2 Muthukrishnan-Stroud gates (M-S gates)

Muthukrishnan and Stroud proposed a primitive 2×2 quantum controlled gates in multivalued logic which can be used in reversible/quantum ternary circuit design [12]. Figure 2 illustrates the schematic design of an M-S gate. As can be seen in this Figure, A and B are inputs and P and Q are outputs. One of the inputs in M-S gate is the controlled input (A). Only if the controlled input A=2, Q is the Z-transformation (where Z= +1, +2, 01, 02, 12) of the input B, otherwise, Q=B. The quantum cost attributed to this gate is 1 [11].

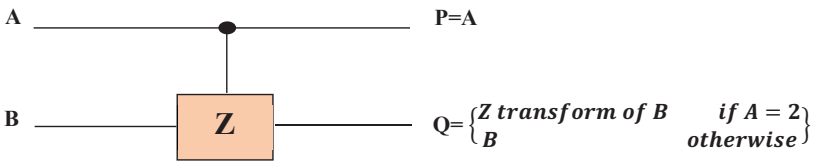

Fig. 2 The symbol of 2×2 Ternary Muthukrishnan-Stroud Gate [11, 12]

4 The ternary numeral system

To implement the reversible arithmetic operations on integer numbers in ternary logic, a specific number representation is required. In this paper, the 2-tuple is used to represent integer numbers. Each of the elements of the 2-tuple is called trit (ternary digit). A trit can be one of the digits 0, 1 or 2. Therefore, only $3^2=9$ numbers can be represented with 2-tuple of trits. In this section, first, the integer numbers representation without considering a sign is given, then, by considering the sign, the numeral system used in this article for representing the positive and negative numbers is presented [8].

4.1 The unsigned ternary numbers representation

The numbers representation in ternary logic is possible with three digits of 0, 1 and 2. For each number expressed in base 3, the place value of the digits is based on the power of 3. The following equation casts light on how to put an integer in the base 10 to base 3.

$$(N)_{Base10}=a_{n-1}\times 3^{n-1}+...+a_2\times 3^2+a_1\times 3^1+a_0\times 3^0 \quad (1)$$

If n-tuple of trits is used to represent the integer numbers, there would be different 3^n code words. If only the representation of unsigned numbers is desired, all the code words can be used to represent the numbers from 0 to 3^n-1. In these ternary codes, the most significant trit does not represent the positive or negative sign. Table 4 represents unsigned integer numbers for 0 to 8 using 2-tuple of trits.

4.2 The signed ternary numbers representation

There exists a number of methods for negative integers representation in base 3. These include the sign-magnitude, 3's complement, and 2's complement. The 3'complement system is used to represent the signed numbers in this paper. Consistent with this system, a negative number is represented using

Table 4 Unsigned ternary numbers representation

Ternary code	Decimal unsigned number
00	0
01	1
02	2
10	3
11	4
12	5
20	6
21	7
22	8

the 3's complement of its positive number code. To calculate the 3's complement for a number in the ternary system first, the 2's complement must be obtained by subtracting its digits from 2. And then, by adding the least significant trit with number 1, the correct code in the 3's complement system for the desired number can be obtained.

Consider, for example, the representation of the number (-3) using 3's complement. In this case, the number 3 is first represented as (10) in ternary system. Then, each trit is complemented by converting 2 to 0 and 0 to 2; hence, the result is (12). Finally, "1" is added to the least significant trit position to result in (20). Now, consider the 3's complement representation of number (+4). Since the number is positive, then, it is represented as (11), like the number in the unsigned representation case. In Ternary system, unlike the binary system, the codes defined in the 3'complement system are completely symmetric around zero. Consequently, with n digits in the 3'complement system, the numbers range of $-(3^n-1)/2$ and $+(3^n-1)/2$ can be represented.

Table 5 shows the numbers represented in the -4 to +4 range in the 3'complement system. In the 3'complement system, if the most significant trit equals 2, the code is related to a negative number, but if it is equal to 1, then, if only after considering all 1s to the lower digits, we reach 2, the code is a negative number. So the code (12) in the 3'complement system is related to -4, while the code (11) corresponds to +4.

Table 5 The signed ternary numbers representation

3'complement ternary code	Decimal signed number
00	0
01	1
02	2
10	3
11	4
12	-4
20	-3
21	-2
22	-1

5 The Ternary logic addition / subtraction

In this section, the techniques applied in this paper for the reversible addition / subtraction of two 2-trit ternary numbers are explained first for the unsigned numbers; and subsequently, for the signed numbers. Also, the conditions for the overflow existence as a result of computation are investigated. The overflow in calculation occurs when the result of the addition or subtraction calculation is a number that is not defined in the range of numbers represented in the code book. In this case, the result is not correct [8].

5.1 The unsigned 2-trit addition/subtraction

To add two 2-trit unsigned ternary numbers, the corresponding trits are added without giving a special treatment to the signed bit. For example, the result of adding two numbers of (10) and (12) produces (22). In this case, the overflow will occur when the result is more than decimal number 8. In such a situation, having an output carry number can detect overflow. For example, the result of the addition of (12) and (20) is equal to 00 with a value of 1 in the output carry. So, the result is invalid due to the overflow occurrence.

The subtraction of two unsigned ternary numbers can be calculated by adding the minuend with the 3's complement of the subtrahend. In this case, the 3's complement representation of a negative number is used. The main advantage of the 3's complement representation is that no special treatment is needed for signing the numbers. If a carry number, coming out of the most significant trit while performing subtraction operation, is equal to 1, the result is positive and the output carry number is ignored without affecting the correctness of the result, otherwise, the result is a negative number and we should correct it by computing 3's complement of the obtained sum to get a valid ternary code. Consider the following two examples.

Example 1. Consider subtracting number 6 (20) with number 4 (11). The result will be 2 (01) and the output carry number is 1. So, the result is correct (+2) if the carry bit is ignored.

Example 2. Consider the subtraction of $3-6=-3$. The subtraction can be done as $(3)+(-6)=(-3)$, that is, (10) + (not (20) +1) = (20), a negative result. This is because the output carry number is 0. Therefore, (20) is a negative number in 3's complement codes. To reach the valid ternary code in unsigned numbers range, the 3's complement of the result should be re-calculated. Therefore, the valid answer is - (10). In the subtraction of two unsigned numbers, there will never be an overflow.

5.2 The 2-trit signed addition/subtraction

In this paper, 3's complement system is used to represent the signed numbers, accordingly, in this section, a description of 3's complement addition/subtraction will be provided. The addition of two 2-trit signed ternary numbers in 3's complement system can be performed using a 2-trit ternary adder. Any carry-out trit can be ignored without affecting the correctness of the results. An overflow will occur if the result produced by a given operation is outside the range of the representable numbers. So, a result outside "-4 to +4 "range will lead to an overflow, and hence, will be a wrong result. Consider the following example.

Example 1. Consider adding the two numbers of (-4) and (-3). The addition can be done as 3's complement of (+4) and (+3), that is (12) + (20) = (02), which is a wrong result. This is because the result is less than the lowest value (-4) in range of representation numbers.

It can be concluded, from the above example, that if both numbers that are added have similar signs, but the result of the addition has the sign opposite to them, there is an overflow. In 3's complement, the subtraction can be performed in the same way the addition is performed. It should be noted that our earlier observation about the occurrence of overflow in the context of addition applies in the case of subtraction, as well.

Example 2. Consider the subtraction of (-3)-(2) = (-1), this can be performed as (-3) + (3's complement of 2) = (20) + (21) = (11) which is a wrong result. The result is a positive number while the added numbers have been negative numbers. This is because of the overflow occurring.

6 Our proposed reversible circuits

In this section, the circuits for reversible parallel addition/subtraction of two 2-trit signed/unsigned integers are proposed. Subtracting two 2-trit signed/unsigned integer numbers can be performed by the addition of 3's complement of the subtrahend to the minuend. Besides, the addition and subtraction operations for the two A, B numbers, the presented computational circuits are also capable of performing A-1, A+1, A+B+1 and A-B-1 calculations. Also, in this section, a new module for identifying overflow is designed and by applying it in the proposed computational circuit, for two 2-trit signed ternary numbers, the overflow detection capabilities are provided in this circuit. To implement all proposed circuits, 1-qutrit shift gates and 2-qutrit Muthukrishnan-Stroud (MS) gates which are realized in ion-trap technology in quantum computers were used.

6.1 Our proposed reversible 2-trit unsigned ternary adder

In this subsection, the optimal circuit for reversible parallel addition of two 2-trit unsigned numbers is proposed. The proposed adder realization is shown in Fig. 3. As seen in this Figure, A (A_1A_0), B (B_1B_0) and C_{in} are inputs and S (S_1S_0) and C_{out} are the main outputs. The MS gates number used in this circuit implementation is 20 and the number of shift gate is 3, resulting in a quantum cost of 23 in the circuit. To implement this adder, only one constant input is used and the input carry value is considered to be 0 and 1. Our proposed reversible 2-trit adder has less quantum cost and constant inputs in

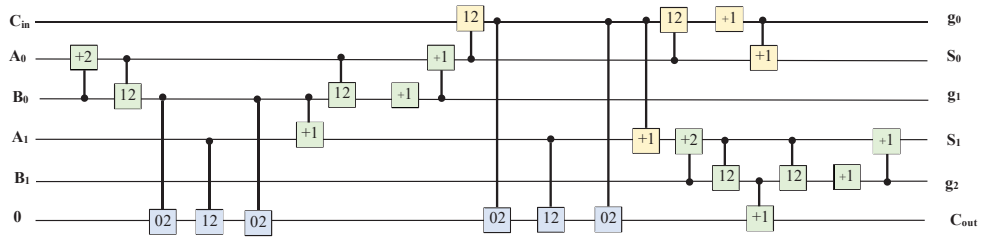

Fig. 3 The implementation of the proposed reversible 2-trit unsigned ternary adder

Table 6 All mathematical operations that can be done by the circuit proposed in Fig.4.

S	C_{in}	Input A	Input B	Operation
0	0	A	B	A+B
0	1	A	B	A+B+1
0	1	A	(00)	A+1
0	0	A	(22)	A-1
2	0	A	B	A-B
2	1	A	B	A-B-1

comparison with suggested parallel adders in [11,17,19,21,22,24,25]. In our proposed parallel adder, if the value of output carry equals 1, then, the overflow occurs and the result would be an invalid answer.

6.2 Our proposed reversible 2-trit unsigned ternary arithmetic unit

In this subsection, we propose the reversible 2-trit unsigned adder/subtractor circuit. Our proposed circuit is shown in Fig.4. Table 6 presents all the mathematical operations that can be done by this circuit. The S and C_{in}/B_{in} inputs are used to select the desired operation in the circuit provided. If the value 0 is selected for input S, the circuit presented in this section will become an adder and will have a function similar to the circuit in Fig. 3. To subtract two numbers of A and B, the value of S and C_{in} should be equal to 2 and 0, respectively. In this situation, the integer B 3's complement is calculated first, and then, the result is added with A.

In the subtraction of A-B, if A > B, the result is a positive number. In this case, the Sign/B_{out} output will be 0, and the subtraction result will be in the unsigned numbers range of 0 to 8. And if A<B, then, the result is a negative number and the resulting code is a negative numerical code in the 3's complement representation. The Sign/B_{out} value will be 1 in this case. Accordingly, to get the correct code in the unsigned numbers range of 0 to 8, the 3's complement of the result must be recalculated.

In the specified computational circuit, the input numbers are in 0 to 8 range, and the result obtained consistent using the correct circuit will always be in the 0 to 8 range. The sign output is used to indicate the result sign of the calculation. If the output sign value is 0, the result is a positive integer and if the sign is equal to 1, the result is a negative number. There will be no overflow in the subtraction of two unsigned integers and the result of the subtraction will always be a number between 0 and 8. 36 MS gates and 7 shift gates were used for this circuit implementation. Also, 2 inputs had a constant value of 0.

6.3 Our proposed reversible 2-trit signed ternary arithmetic unit

Our provided circuit, in this subsection, is used for the addition/subtraction of two signed numbers. Figure 5 shows our proposed reversible ternary arithmetic circuit implementation. The operation of this circuit is similar to the circuit shown in Fig. 4 holding the difference that the inputs and outputs of the circuit in Fig. 4 are the unsigned numbers ranging from 0 to 8; while the inputs and outputs in the circuit presented in this section can be positive and negative numbers in the -4 to +4 range.

In this circuit, the 3's complement representation is used to represent the input numbers. And the subtraction of two A, B numbers is conducted regardless of considering B number sign with 3's complement. The obtained code for the result of subtraction or addition happens to be in the 3's complement system. Codes related to numbers in -4 to +4 range in the 3's complement system were listed in Table 5. The inputs and outputs of the circuit in Fig. 5 are based on the codes in Table 5.

Like the circuit in Fig. 4, the circuit provided in this section also performs all the six calculations given in Table 6 for the signed numbers in the 3's complement system. Considering this circuit im-

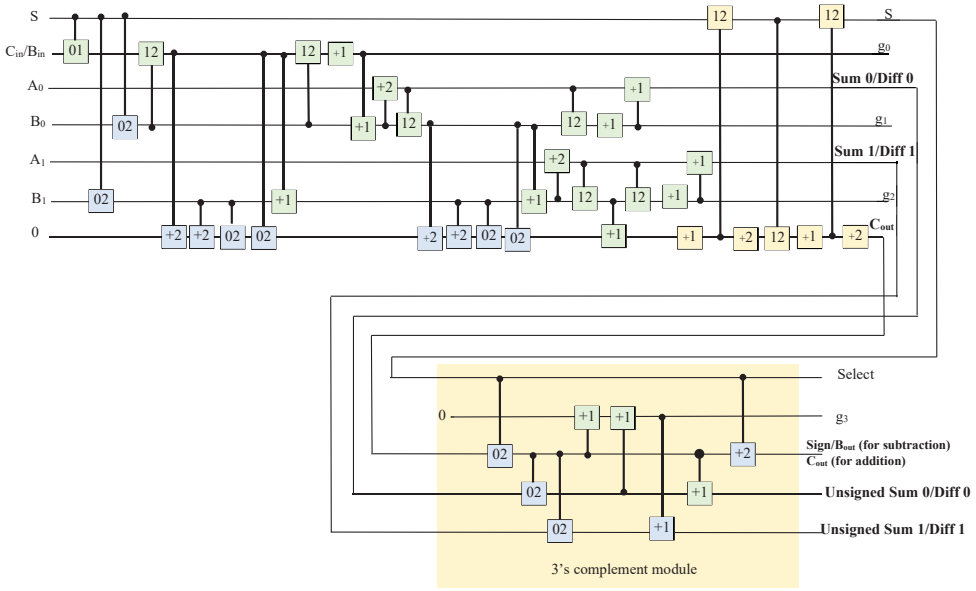

Fig. 4 The implementation of the reversible 2-trit unsigned ternary arithmetic unit

plementation, 27 MS gates and 5 shift gates were used. Accordingly, the quantum cost is 32. Moreover, in the implementation of this circuit, only a constant input with zero value is used.

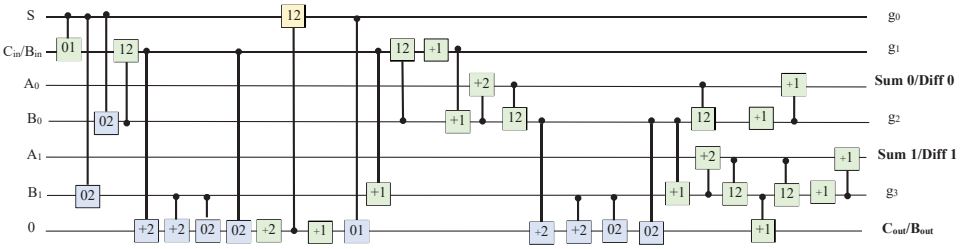

Fig. 5 The implementation of the reversible 2-trit signed ternary arithmetic unit

6.4 Our proposed reversible overflow detection module

In this section, we present a novel reversible ternary module to detect the overflow in the signed numbers addition and subtraction calculation. Since the signed numbers in the article are represented in the 3's complement system and the subtraction of the two signed numbers is performed using the addition, in this case, if the sum of the two numbers with the same sign is the opposite of the result, the overflow has occurred and the calculation result is a number that cannot be represented in the numbers range in the 3's complement system. Accordingly, the module presented in Fig. 6 identifies the presence or absence of overflow by checking the sign of the input numbers and the result sign of the addition. In Fig. 6 , if the overflow output has a value of 2, the overflow has occurred in the calculation and the result is invalid. In the module provided for the overflow detector, three sign detector blocks were used.

In Table 7 , all possible positions for the two numbers sign and the addition result sign are given. As can be seen in this table, in cases where the sign of both input numbers was the same and opposite to their addition sign, the overflow output value was equal to 2.

The circuit shown in Fig. 7 is related to the design of the sign detector block. In the sign detector circuit, if the output S is equal to 2, the input number is negative, otherwise, the input number is positive. The sign detector circuit is based on the codes in Table 5 for positive and negative numbers in the "-4 to +4" range in the 3's complement system.

In implementing the sign detector circuit, 4 MS gates and 2 shift gates were used, so the quantum cost was 6. Also, a constant input of zero was used in this circuit. In the overflow detector module

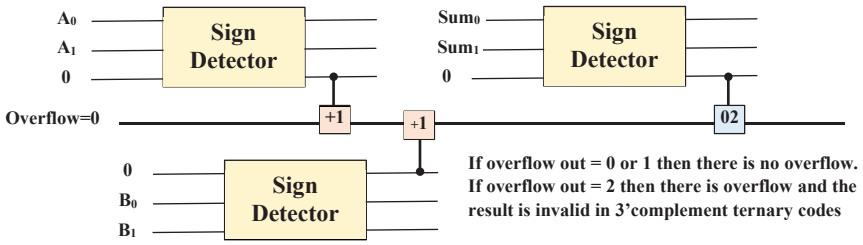

Fig. 6 Our proposed overflow detection module

Table 7 The investigation of overflow in all possible cases for the sum of two numbers

A	B	A+B	The value of overflow output
+	+	+	0
+	+	-	2 *There is overflow
+	-	+	1
+	-	-	1
-	+	+	1
-	+	-	1
-	-	+	2 *There is overflow
-	-	-	0

implementation, three sign detector blocks and a constant input with a zero value were used, and the quantum cost was 21.

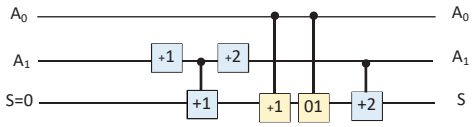

Fig. 7 The implementation of the sign detector module

6.5 Our proposed reversible 2-trit signed arithmetic unit with overflow detection

In this section, by adding the overflow detection module to the computational circuit proposed in Fig. 5, a new circuit for addition and subtraction calculations for positive and negative numbers in the 3's complement system capable of detecting the invalid result in case of overflow is presented. The circuit presented here provides all the calculations in Table 6 being able to detect the overflow for signed numbers. In the proposed circuit, if the overflow output is set to 2, the resulting code is not related to the result of the calculation and the overflow occurs. In such a situation, the numerical calculation result is not between -4 and +4. In the implementation of this circuit, 59 MS gates and 21 shift gates were used. So the quantum cost was 80. It also used 7 constant inputs.

7 Evaluating The results

In this section, we have analyzed the performance of the proposed circuits with the existing similar designs if available. The most important parameters for the reversible ternary circuit design, including the quantum cost, number of constant inputs and garbage outputs, are used to evaluate the given circuits. Designing with lower values for these parameters will lead to a more optimal circuit.

7.1 Evaluating the proposed reversible 2-trit unsigned Ternary Adder

Table 8 shows the comparison between our proposed reversible 2-trit unsigned ternary adder circuit and the existing similar designs in Refs. [11, 17, 19, 21, 22, 24, 25] in terms of quantum cost, the number

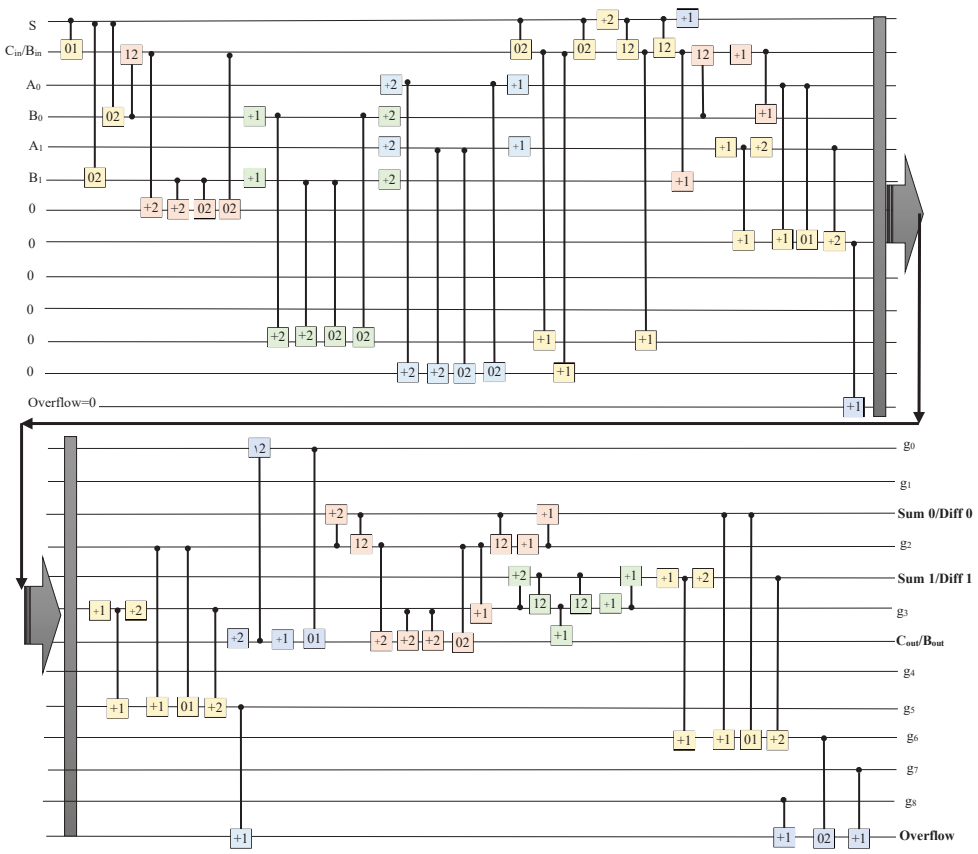

Fig. 8 The implementation of the reversible 2-trit signed arithmetic unit with overflow detection

of primitive gates, constant inputs, and garbage outputs. As can be witnessed in Table 8, our proposed circuit has less quantum cost, constant inputs, and garbage outputs as compared to the rest of the proposed circuits. Therefore, our proposed parallel adder is more efficient. The most important property of our proposed parallel adder is using only one constant input, while other similar designs have used two or more constant inputs.

Table 8 The comparative analysis of the proposed and existing designs for reversible 2-trit unsigned ternary adder circuits

	#Garbage output	#Constant input	#Shift gate	#MS gate	quantum cost
Existing [11]	9	8	28	72	100
Existing [22]	8	6	16	52	68
Existing [19]	4	2	24	28	52
Existing [17]	4	2	8	20	28
Existing [21]	4	2	8	18	26
Existing [24]	4	2	4	20	24
Existing [25]	4	2	4	20	24
This work	3	1	3	20	23

7.2 Evaluating the proposed reversible 2-trit unsigned ternary arithmetic unit

The computational circuit evaluated in this section is suited for the addition and subtraction of 2-trit unsigned ternary numbers and, in comparison with the similar circuits proposed in [11, 19, 22], it has the following unique features.

- Calculating six mathematical operations according to Table 6.
- Using the correction circuit to convert the obtained negative code from 3's complement system to unsigned ternary representation ranging between 0 and 8.
- Assigning one of the outputs (C_{out}/Sign) to the result sign.

Table 9 The analysis of the proposed design for reversible 2-trit unsigned ternary arithmetic nuit

	#Garbage output	#Constant input	#Shift gate	#MS gate	quantum cost
Our proposed circuit	5	2	7	36	43

This is the first time that a circuit with the above features is proposed. Consequently, it cannot be compared with similar circuits. The analysis of the presented computational circuit is given in Table 9.

7.3 Evaluating of the proposed reversible 2-trit signed ternary arithmetic unit

The functioning of our proposed arithmetic unit is similar to the parallel adder/subtractor circuits presented in [11,19,22]. In our proposed circuit, the inputs are positive and negative numbers in the 3's complement system listed in Table 5 and the obtained result is a ternary code in the 3's complement system. The evaluation and comparison of our proposed parallel adder/subtractor with the existing similar circuits is shown in Table 10. As can be seen in this table, in the implementation of the proposed circuit, the quantum cost, constant inputs, and garbage outputs have been used less, compared to similar circuits. So the proposed circuit is more efficient than the existing circuits and has less hardware complexity.

Table 10 The comparative analysis of the proposed and existing designs for reversible 2-trit signed ternary adder/subtractor

	#Garbage output	#Constant input	#Shift gate	#MS gate	quantum cost
Existing [11]	10	9	28	75	103
Existing [22]	9	7	16	55	71
Existing [19]	5	3	24	31	55
This work	4	1	5	27	32

7.4 Evaluating of the proposed reversible overflow detection module

Since the circuit for overflow detection module is proposed for the first time, it cannot be compared to other similar circuits. To implement this circuit, three sign detector blocks and one constant input were used. The evaluations of the circuits proposed for the sign detector block and the overflow detector module are presented in Table 11.

Table 11 The analysis of the proposed reversible sign detector block and overflow detection module

	#Garbage output	#Constant input	#Shift gate	#MS gate	quantum cost
Sign detector block	2	1	2	4	6
Overflow detection module	6	4	6	15	21

7.5 Evaluating of the proposed reversible 2-trit signed arithmetic unit with overflow detection

The proposed circuit evaluation for the 2-trit signed arithmetic unit with overflow detection is shown in Table 12. This circuit is presented for the first time so it cannot be compared with other similar circuits. In implementing this circuit, we have tried to use the minimum quantum cost and the minimum number of constant inputs and garbage outputs.

Table 12 The analysis of the proposed reversible 2-trit signed ternary arithmetic unit with overflow detection

	#Garbage output	#Constant input	#Shift gate	#MS gate	quantum cost
presented circuit	9	7	21	59	80

8 Conclusion

in this paper for the first time, a novel technique for designing signed reversible ternary parallel arithmetic circuit with an overflow detection capability to calculate six mathematical operations of A+B, A-B, A+1, A-1, A+B+1 and A-B-1 on two 2-trit signed ternary numbers on the basis of 1-input shift gates and 2-input MS gates which can be physically implemented in ion-trap technology in quantum computer was proposed. The presented circuit used the new proposed reversible ternary parallel adder with the quantum cost of 23 which had lower-cost in comparison with existing counterparts. Accordingly, the provided signed arithmetic circuit was optimized in terms of Quantum cost, the number of primitive gates, constant inputs and garbage outputs as much as possible. Inputs and outputs in this circuit were represented in the 3's complement system between -4 and +4. Also, in this paper, another computational circuit using the proposed parallel adder for performing six mathematical operations of A + B, A-B, A + 1, A-1, A + B + 1 and A-B-1 on two 2-trit unsigned ternary numbers was proposed. In this circuit, using the correction circuit, the calculation result was the same as the inputs in the unsigned ternary representation between 0 and 8.

9 Availability of data and materials

The author declares that the data supporting the conclusions of this article are available within the article.

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